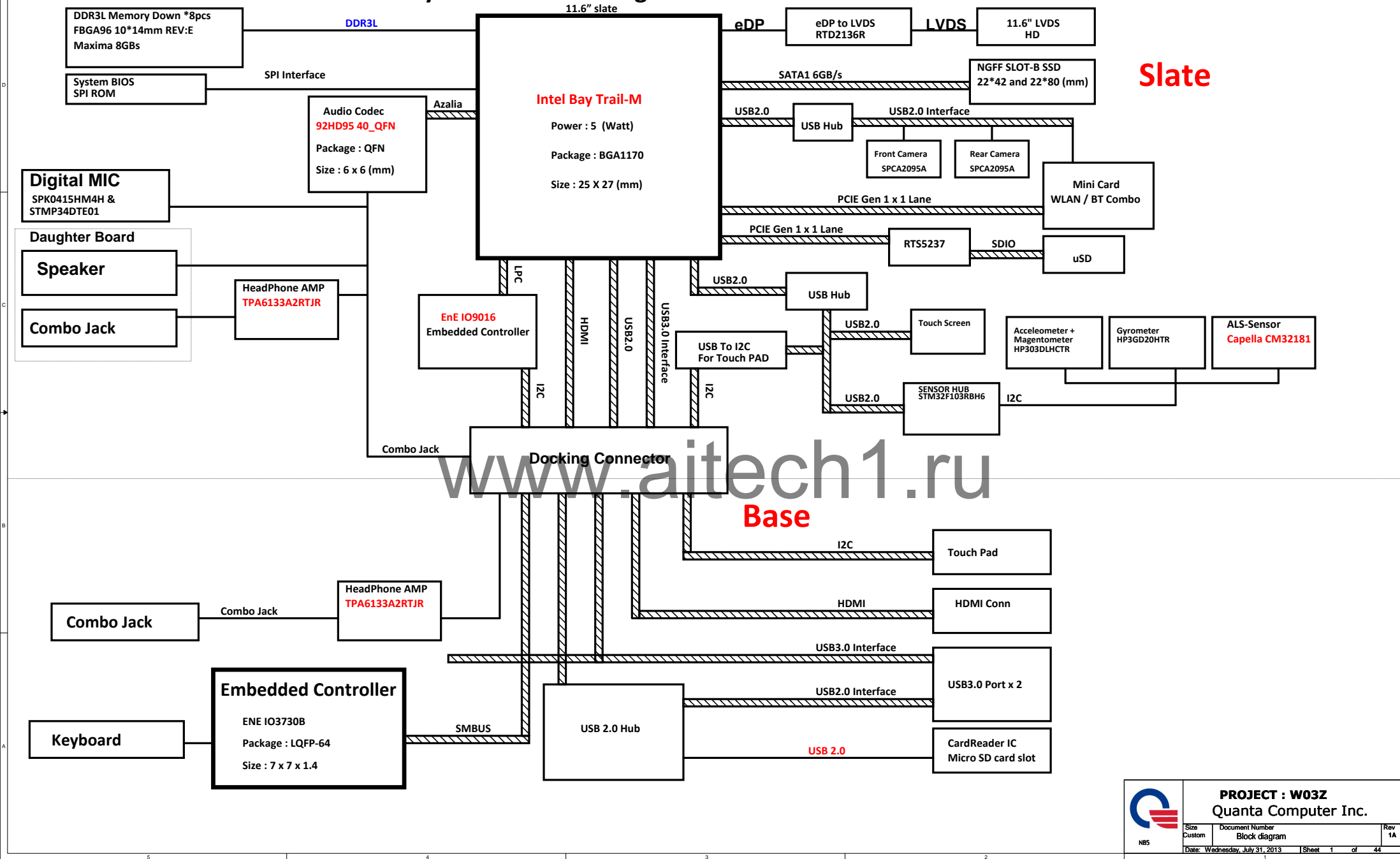
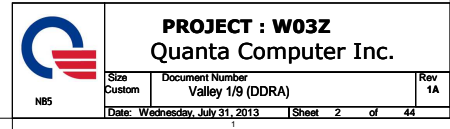
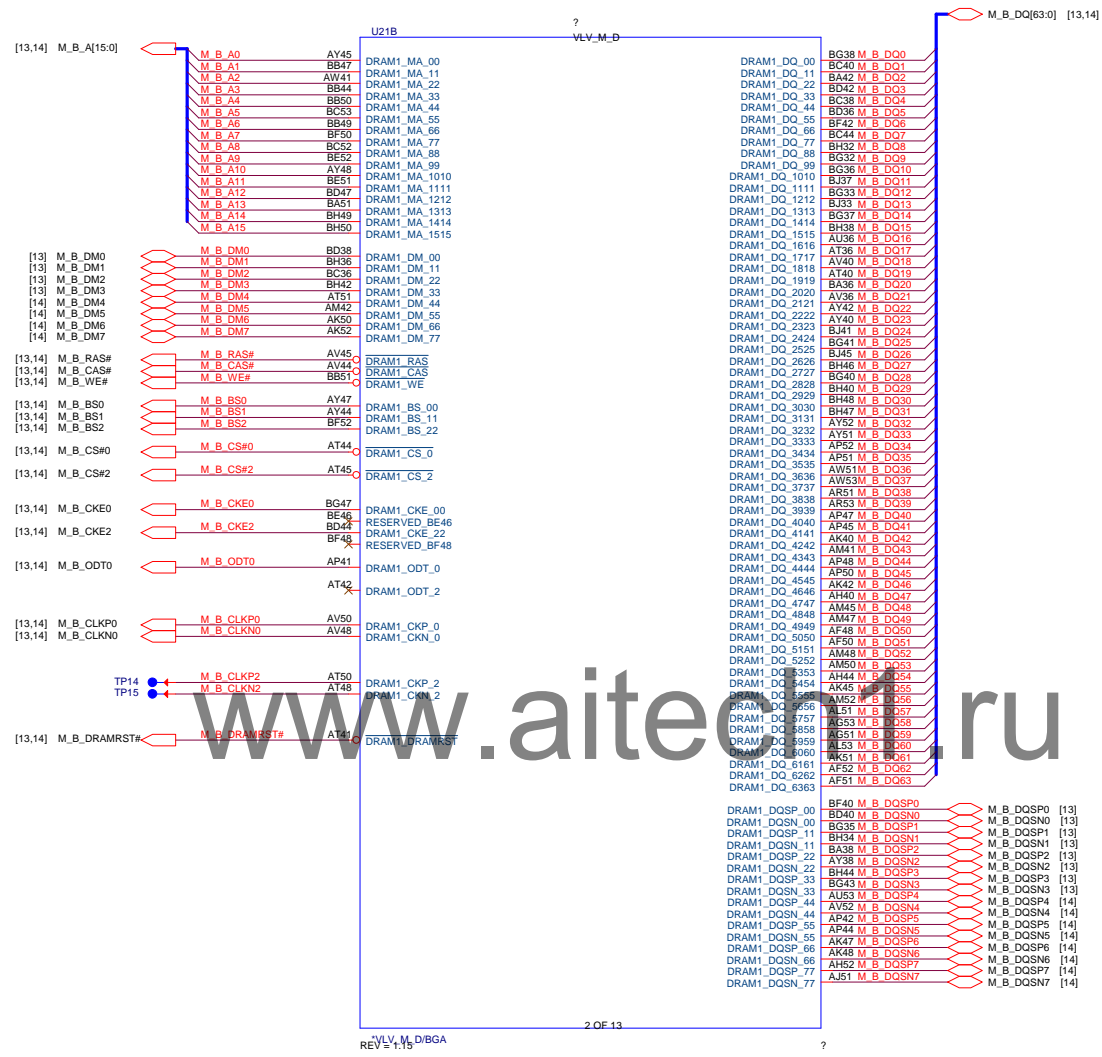
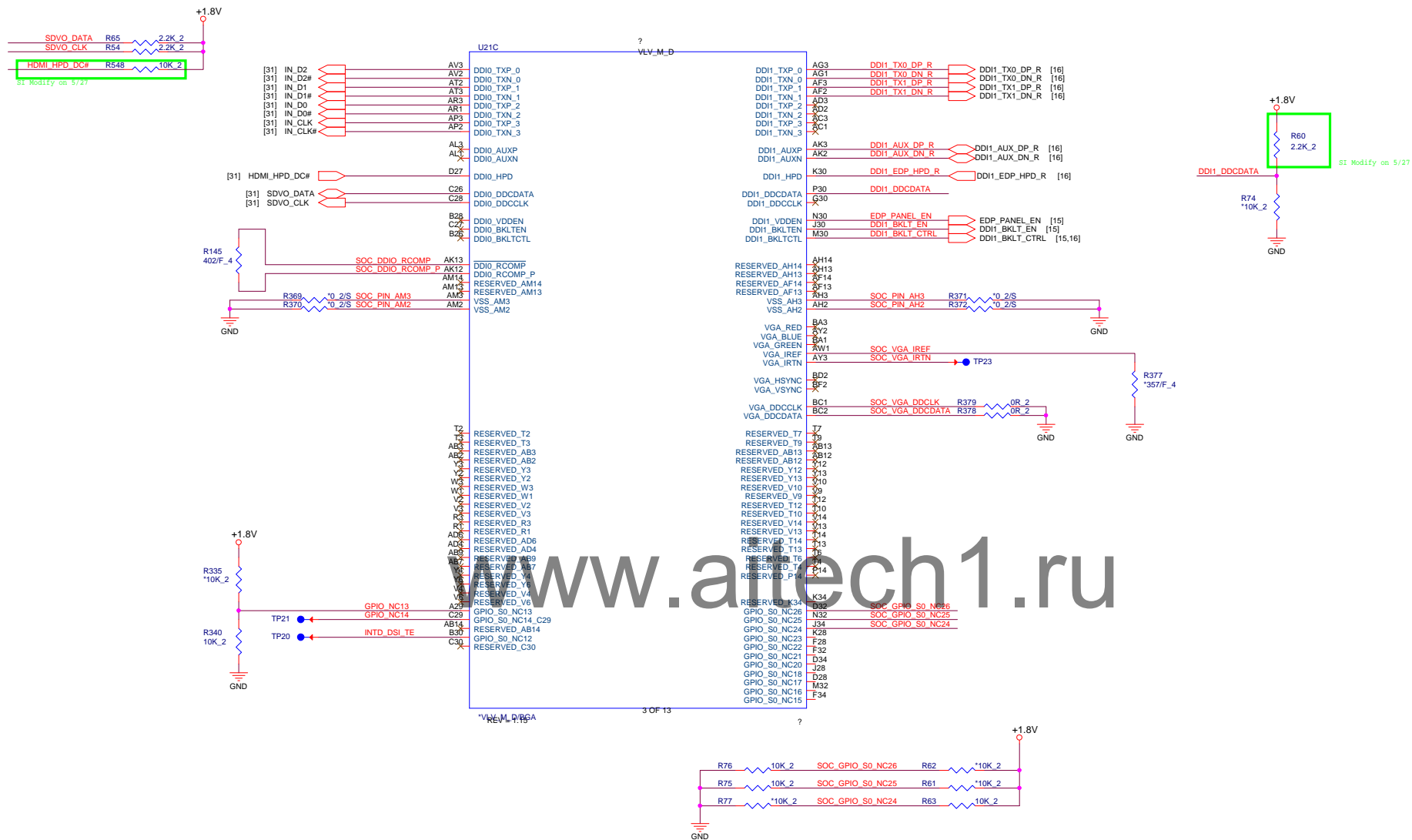


Intel Bay Trail-M Block Diagram

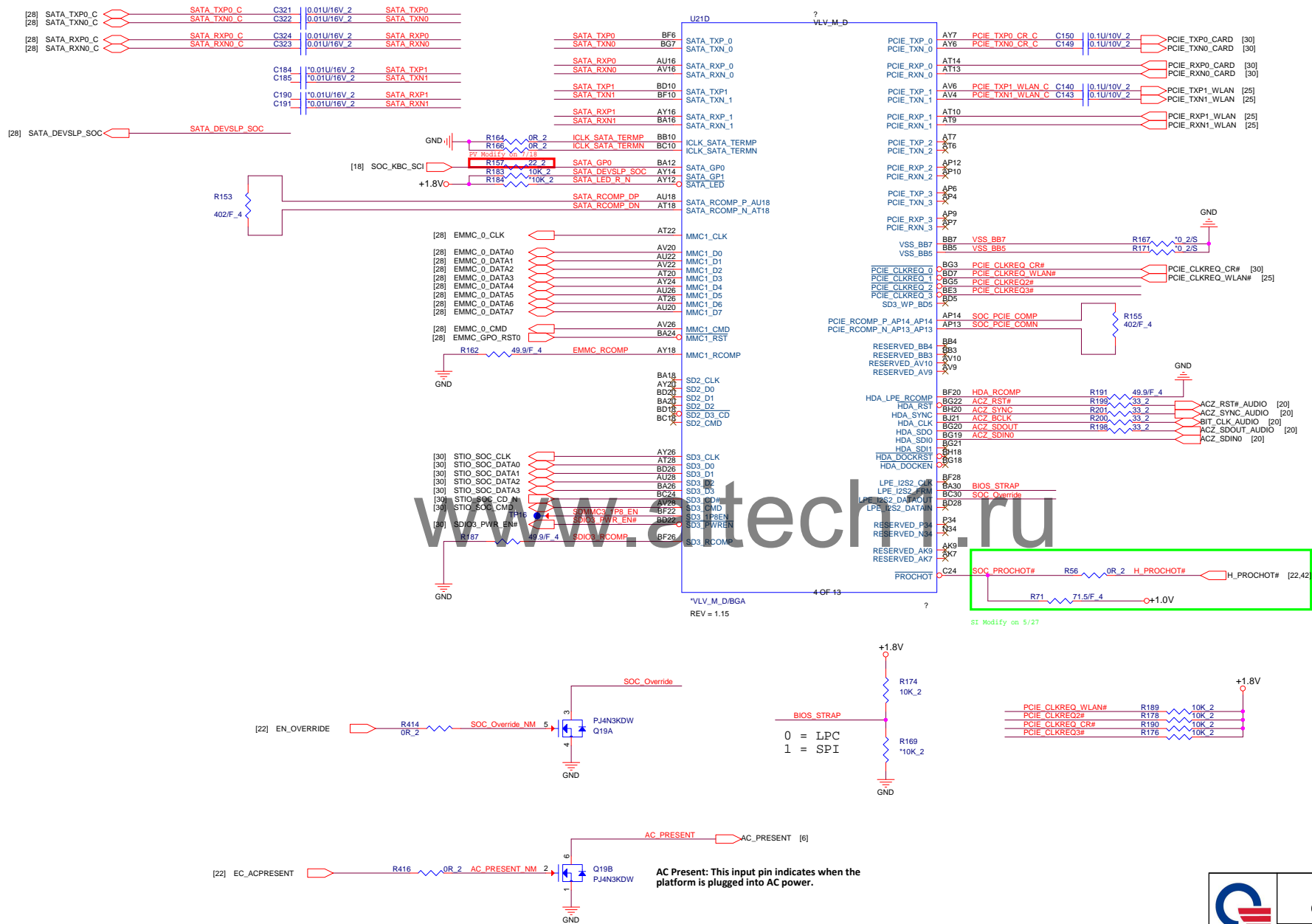


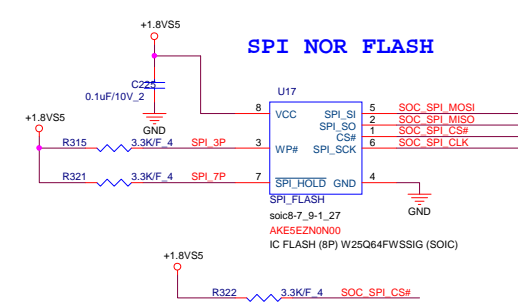
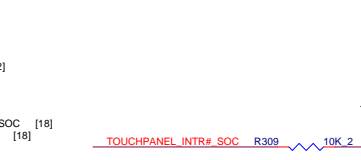
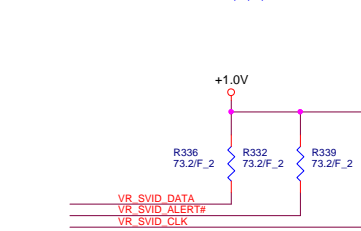
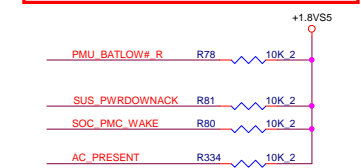





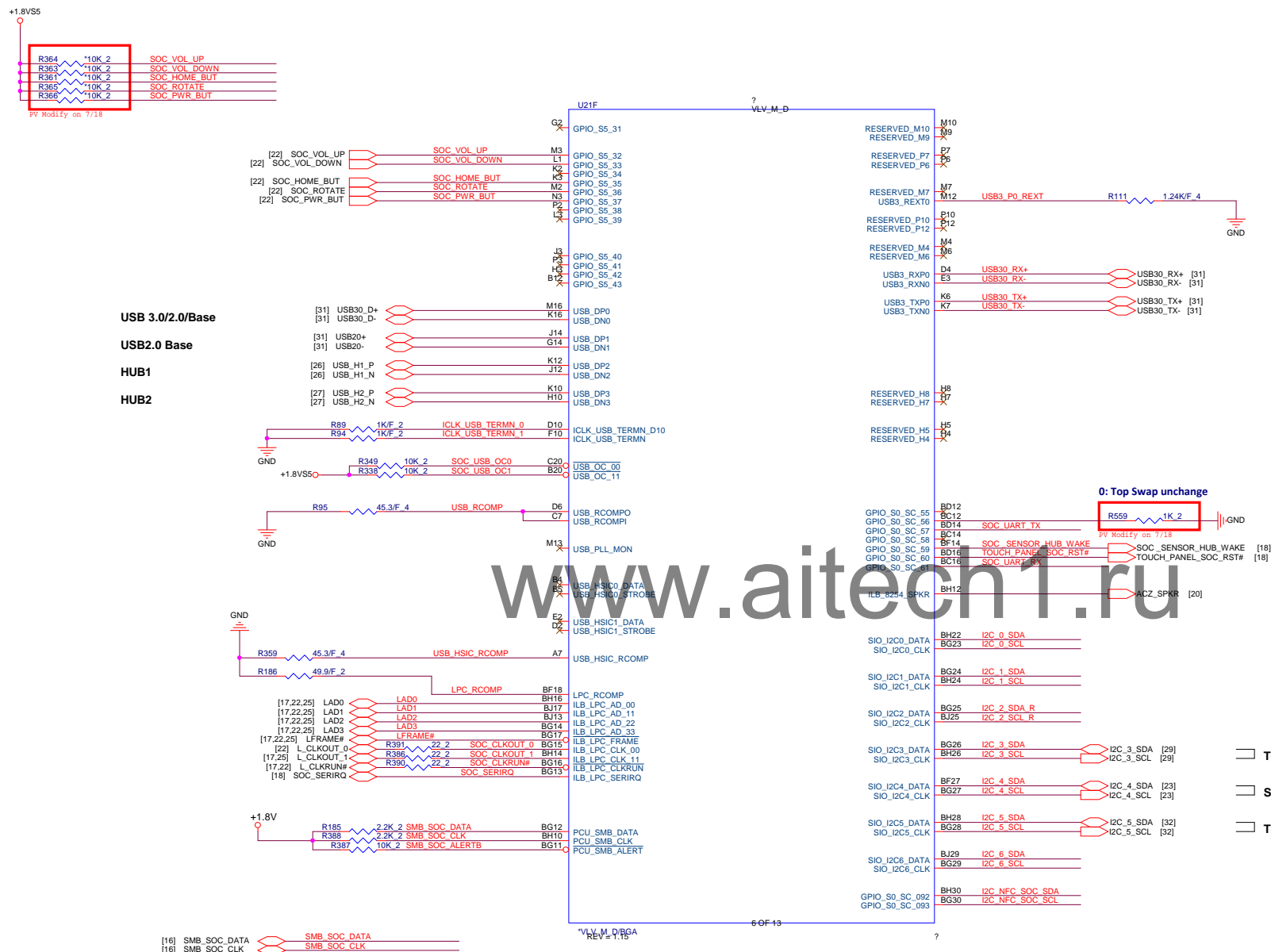


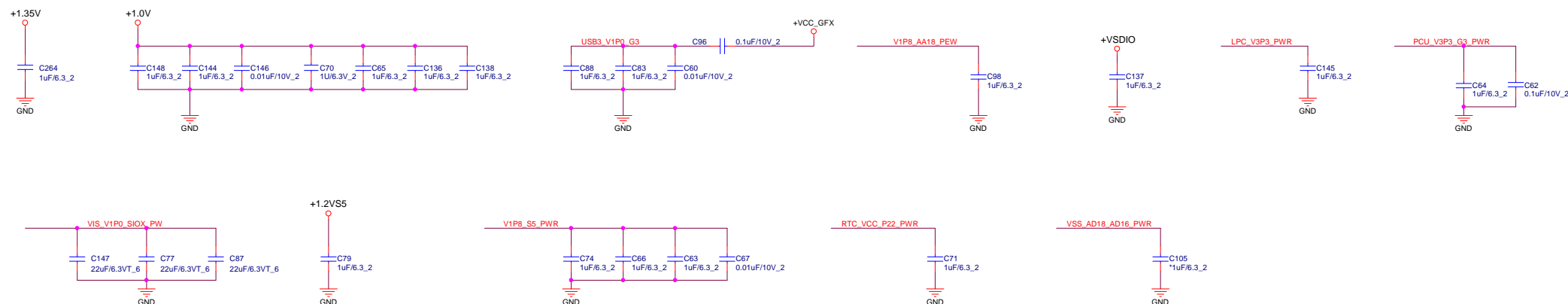
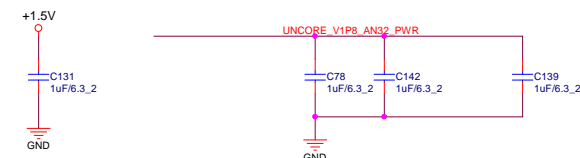
| | 0=4G 1=2G GPIO26 | GPIO25 | GPIO24 | PN |
|--|------------------------|--------|--------|--|
| Hynix (TG) H5TC4G63AFR-PBA HUMA, A | 0 | 0 | 0 | TOPBSQ(AKD5JGETW07)/QBCON(AKD5JGETW08) |
| Micron (TF) MT41K256M16HA-125:E V80A/E | 0 | 0 | 1 | TOPBSQ(AKD5JGSTL06)/QBCON(AKD5JGSTL07) |
| Elpida (TN) EDJ4216EPBG-GN-F F | 0 | 1 | 0 | TOPBSQ(AKD5JGST412)/QBCON(AKD5JGST413) |
| | | | | |
| | | | | |





| | | | |
|--|--|--|-----------|
|  NB5 | PROJECT : W03Z Quanta Computer Inc. | | |
| | Size Custom | Document Number Valley 5/9 (SPI/GPIO/CLK) | Rev 1A |
| | Date: Wednesday, July 31, 2013 | Sheet 6 of 44 | |

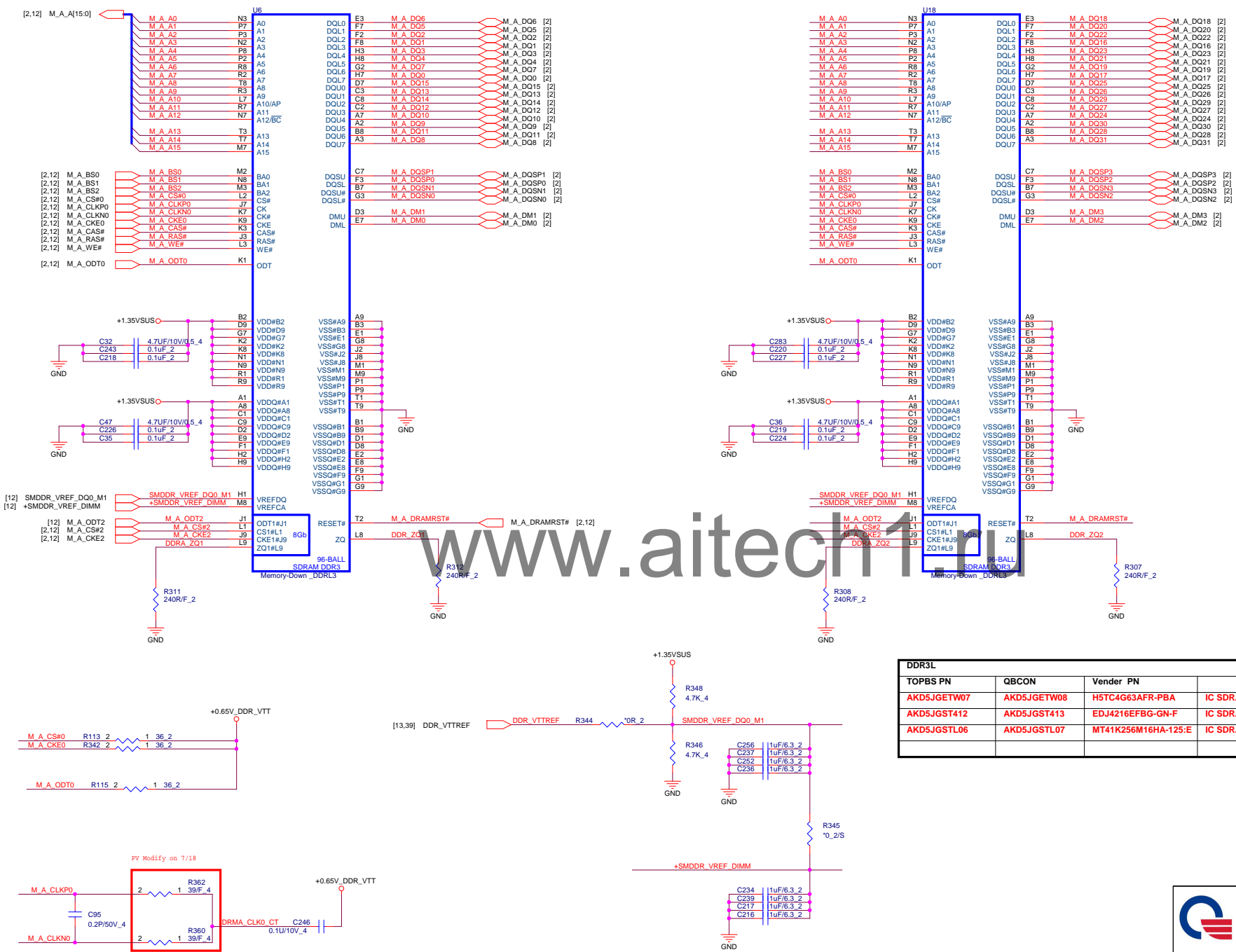


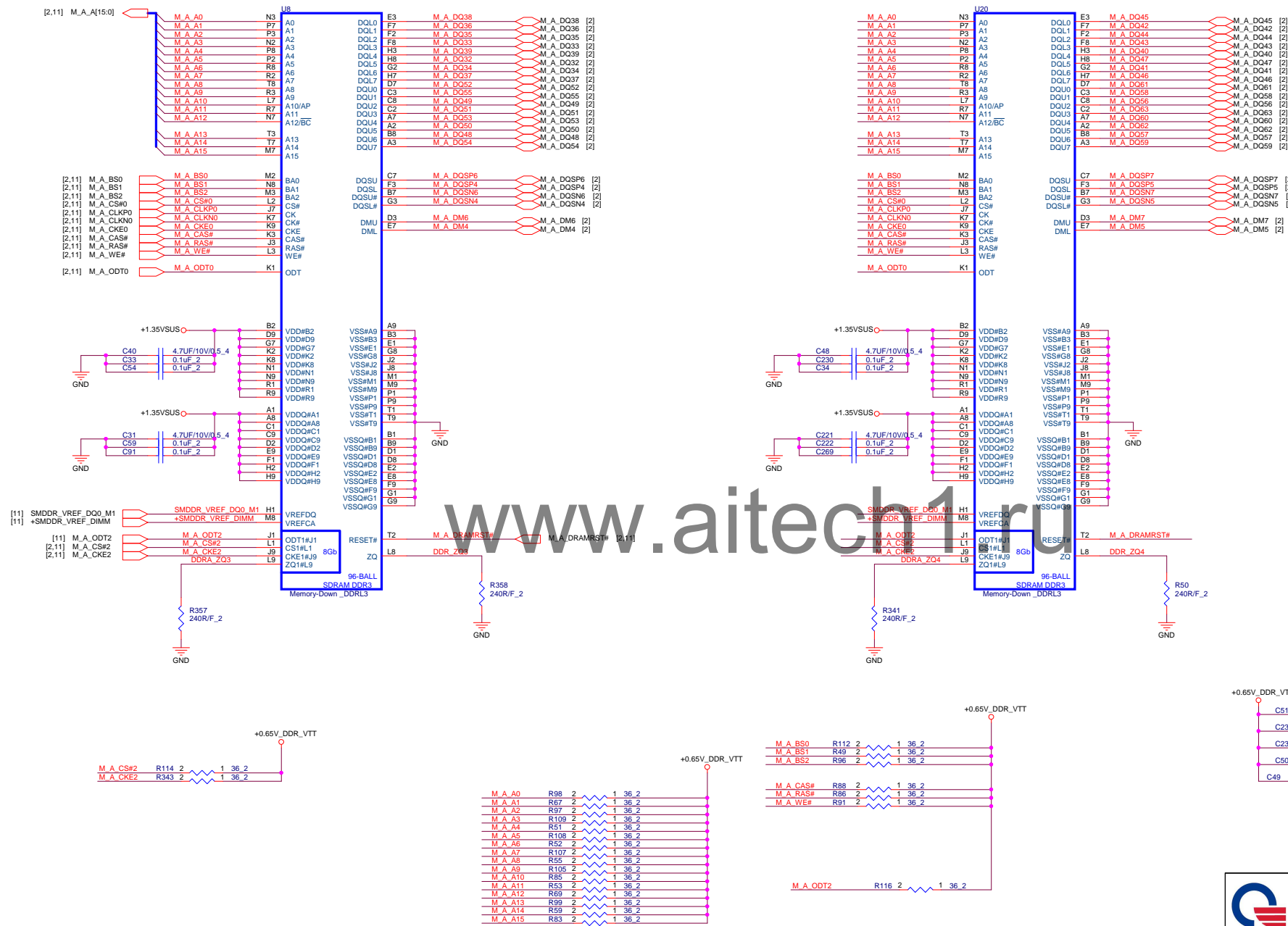


| | | |
|--------------------------------|---|---------------|
| Size Custom | Document Number Valley 8/9 (Power 2) | Rev 1A |
| Date: Wednesday, July 31, 2013 | | Sheet 9 of 44 |



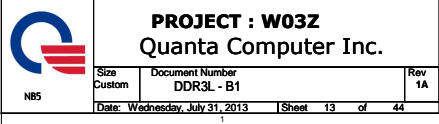
www.aitech11.com

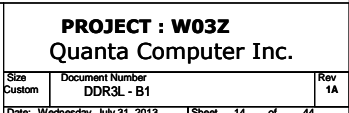
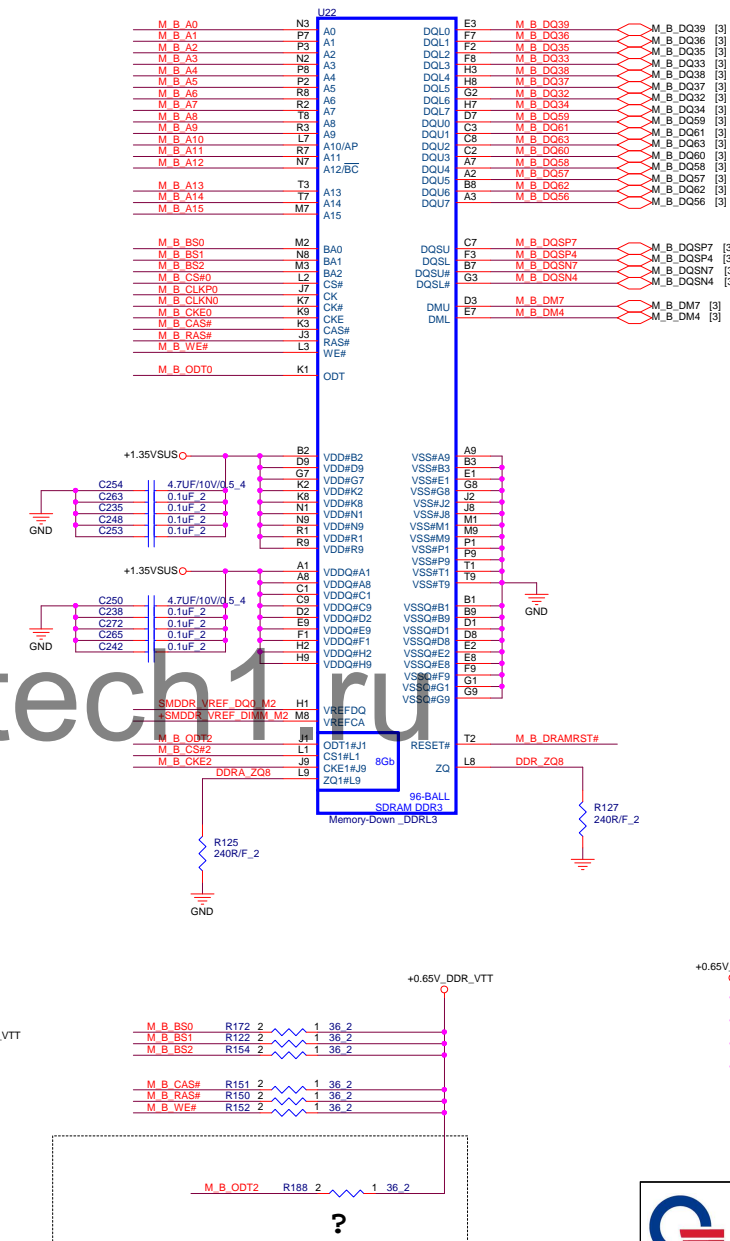




PROJECT : W03Z
Quanta Computer Inc.

| Size | Document Number | Rev |
|--------------------------------|-----------------|-----|
| Custom | DDR3L - A2 | 1A |
| Date: Wednesday, July 31, 2013 | Sheet 12 of 44 | |





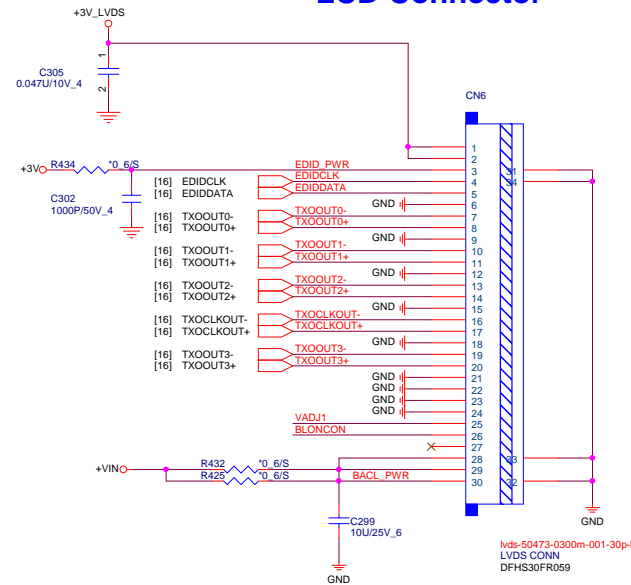
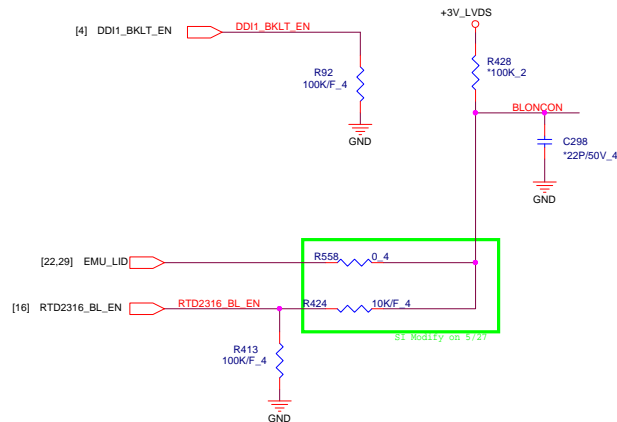
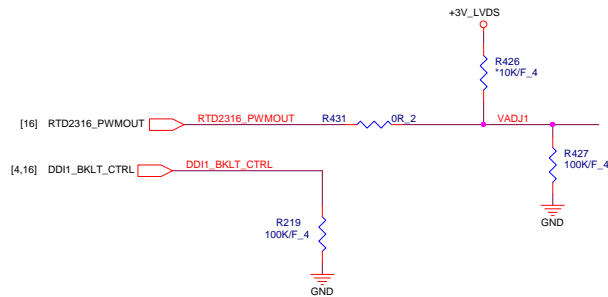
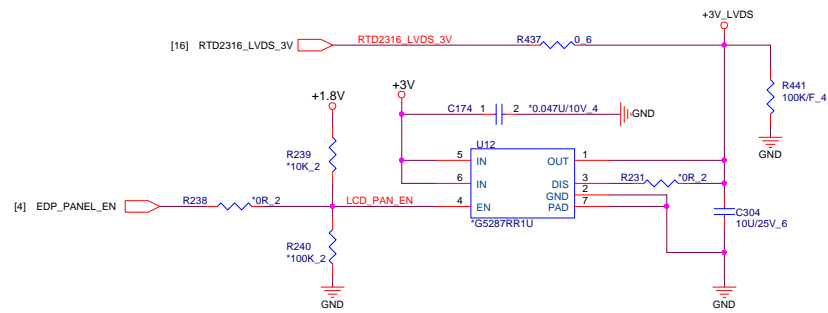


Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

| Pin# | Symbol | Description | Notes |
|------|------------|--|-------|
| 1 | NC | No Connection | |
| 2 | VCC | LCD Logic and driver power (3.3V Typ.) | |
| 3 | VCC | LCD Logic and driver power (3.3V Typ.) | |
| 4 | V EEDID | DDC Power (3.3V) | |
| 5 | NC | No Connection | |
| 6 | CLK EEDID | DDC Clock | |
| 7 | DATA EEDID | DDC Data | |
| 8 | ORX0- | Negative LVDS differential data input | |
| 9 | ORX0+ | Positive LVDS differential data input | |
| 10 | GND | LCM Ground | |
| 11 | ORX1- | Negative LVDS differential data input | |
| 12 | ORX1+ | Positive LVDS differential data input | |
| 13 | GND | LCM Ground | |
| 14 | ORX2- | Negative LVDS differential data input | |
| 15 | ORX2+ | Positive LVDS differential data input | |
| 16 | GND | LCM Ground | |
| 17 | ORX3- | Negative LVDS differential clock input | |
| 18 | ORX3+ | Positive LVDS differential clock input | |
| 19 | GND | LCM Ground | |
| 20 | ORX4- | Negative LVDS differential data input | |
| 21 | ORX4+ | Positive LVDS differential data input | |
| 22 | GND | LCM Ground | |
| 23 | NC | No Connection | |
| 24 | NC | No Connection | |
| 25 | GND | LCM Ground | |
| 26 | NC | No Connection | |
| 27 | NC | No Connection | |
| 28 | GND | LCM Ground | |
| 29 | NC | No Connection | |
| 30 | NC | No Connection | |
| 31 | GND | LCM Ground (LED Backlight Ground) | |
| 32 | GND | LCM Ground (LED Backlight Ground) | |
| 33 | GND | LCM Ground (LED Backlight Ground) | |
| 34 | NC | No Connection | |
| 35 | PWM | System PWM signal input for dimming | |
| 36 | LED_EN | LED Backlight On/Off | |
| 37 | NC | No Connection | |
| 38 | VLED | LED Backlight Power (5V-21V) | |
| 39 | VLED | LED Backlight Power (5V-21V) | |
| 40 | VLED | LED Backlight Power (5V-21V) | |

Interface Chip

1. LED: SIW, SIW0683 (LCD Controller)
2. System: SIW LVDS Rx or equivalent
- * Pin to Pin compatible with LVDS

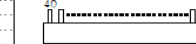
Connector

LSMtron GT05Q-40S-H10, 40 Pin

Mating Connector

20453-040T-0# series or equivalent

Connector pin arrangement



[LCD Module Rear View]

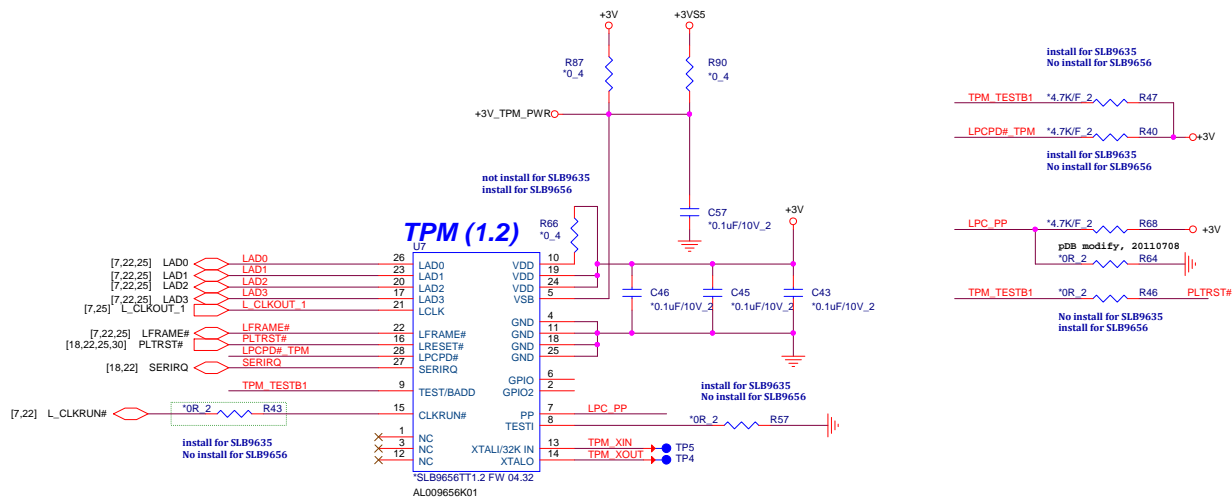
| No. | Pin Name | I/O | Power Rail | Description |
|-----|----------|-----|------------|---|
| 1 | NC | | | No Connection (Reserve) |
| 2 | VDD | | | Power Supply +3.3V |
| 3 | VDD | | | Power Supply +3.3V |
| 4 | VEDID | | | EDID +3.3V Power |
| 5 | AGING | | | Aging Mode Power Supply |
| 6 | CLK EDID | | | EDID Clock Input (3.3V) note2 |
| 7 | DAT EDID | | | EDID Data Input (3.3V) note2 |
| 8 | Rin0- | | | -LVDSdifferential data input(R0-R5,G0) |
| 9 | Rin0+ | | | +LVDSdifferential data input(R0-R5,G0) |
| 10 | GND | | | Ground |
| 11 | Rin1- | | | -LVDSdifferential data input(G1-G5,B0-B1) |
| 12 | Rin1+ | | | +LVDSdifferential data input(G1-G5,B0-B1) |
| 13 | GND | | | Ground |
| 14 | Rin2- | | | -LVDSdifferential data input(B2-B5,HS,VS,DE) |
| 15 | Rin2+ | | | +LVDSdifferential data input(B2-B5,HS,VS,DE) |
| 16 | GND | | | Ground |
| 17 | ClkIN- | | | -LVDSdifferential clock input |
| 18 | ClkIN+ | | | +LVDSdifferential clock input |
| 19 | NC | | | No Connection (Reserve) |
| 20 | Rin3- | | | -LVDSdifferential data input(R6-R7,G6,G7,B6,B7) |
| 21 | Rin3+ | | | +LVDSdifferential data input(R6-R7,G6,G7,B6,B7) |
| 22 | GND | | | Ground-Shield |
| 23 | NC | | | No Connection (Reserve) |
| 24 | GND | | | Ground-Shield |
| 25 | NC | | | No Connection (Reserve) |
| 26 | GND | | | Ground-Shield |
| 27 | NC | | | No Connection (Reserve) |
| 28 | GND | | | Ground-Shield |
| 29 | NC | | | No Connection (Reserve) |
| 30 | NC | | | No Connection (Reserve) |
| 31 | VLED_GND | | | LED Ground |
| 32 | VLED_GND | | | LED Ground |
| 33 | VLED_GND | | | LED Ground |
| 34 | NC | | | No Connection (Reserve) |
| 35 | LED_PWM | | | System PWM Logic Input Level |
| 36 | VLED_EN | | | LED enable input level (2.5V Min) |
| 37 | CABC_EN | | | No Connection (Reserve) |
| 38 | VLED | | | LED Power Supply (5-20V) |
| 39 | VLED | | | LED Power Supply (5-20V) |
| 40 | VLED | | | LED Power Supply (5-20V) |



PROJECT : W03Z
Quanta Computer Inc.

| Size | Document Number | Rev |
|--------------------------------|-----------------|-----|
| Custom | LVDS connector | 1A |
| Date: Wednesday, July 31, 2013 | Sheet 15 of 44 | |

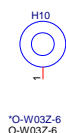
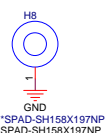
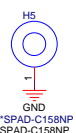
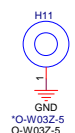
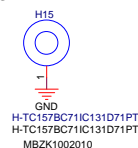
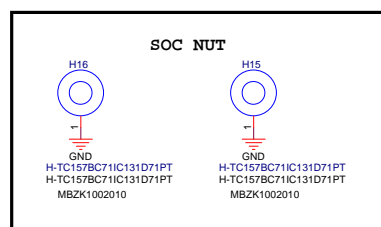
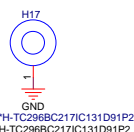
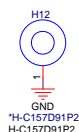
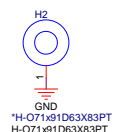
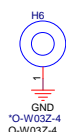
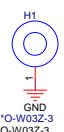
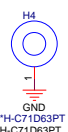
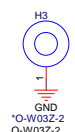
FOR EMI



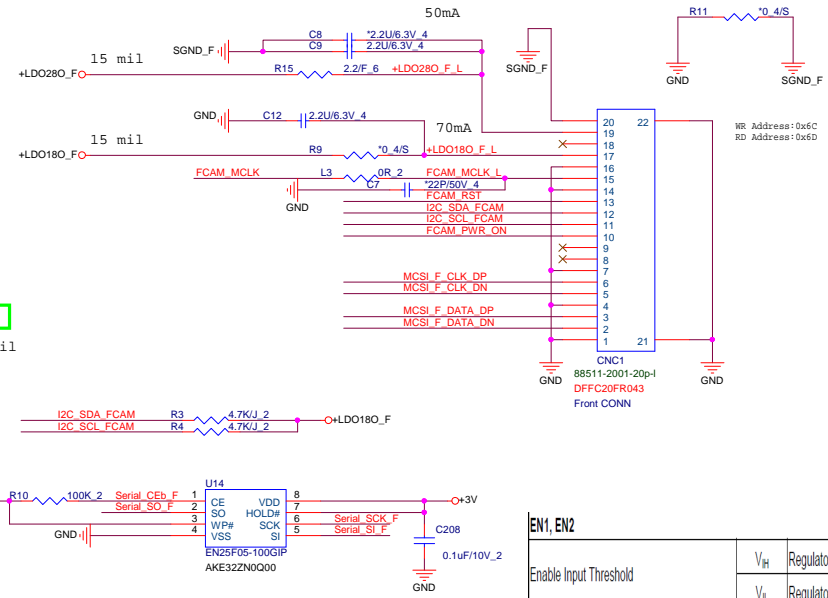
| | SLB9635 | SLB9656 |
|-------|------------|------------|
| R9220 | Install | No install |
| R5446 | No install | Install |
| R5447 | Install | No install |
| R9219 | Install | No install |
| R5448 | Install | No install |
| R5449 | Install | No install |
| R5453 | No install | Install |
| R5458 | No install | Install |

Address

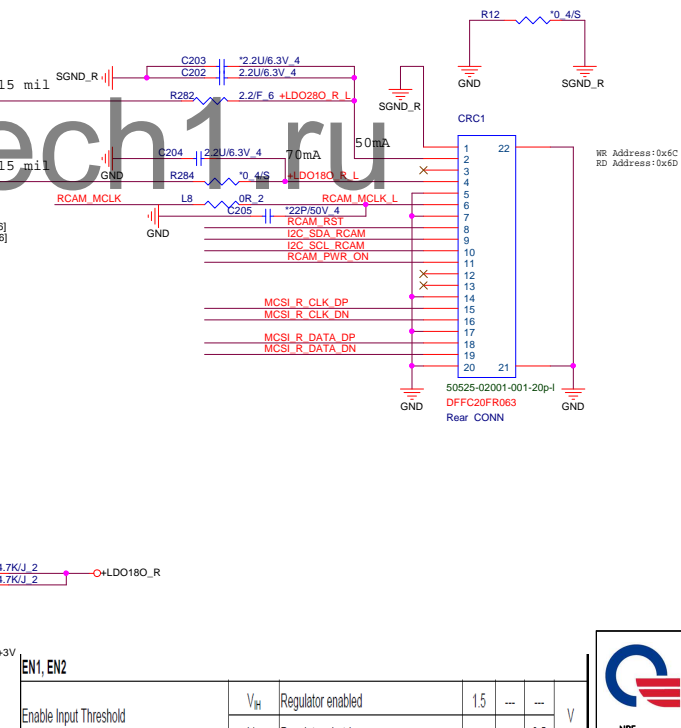
| | BADD |
|------|------------------|
| HIGH | 4EH/4F (default) |







| EN1, EN2 | | | | | | |
|------------------------|-----------------|--------------------|-----|-----|-----|---|
| Enable Input Threshold | V _H | Regulator enabled | 1.5 | --- | --- | V |
| | V _{IL} | Regulator shutdown | --- | --- | 0.5 | |



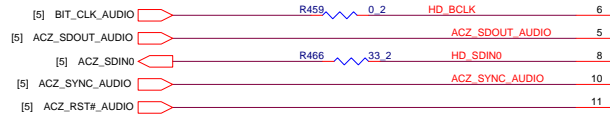
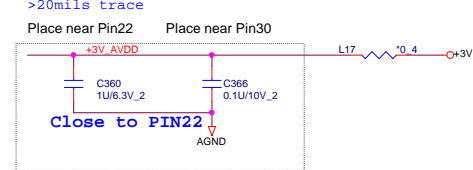
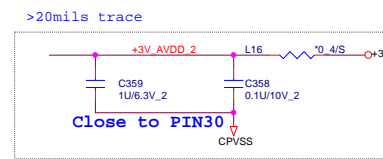
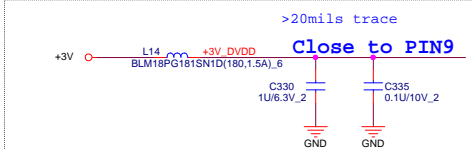
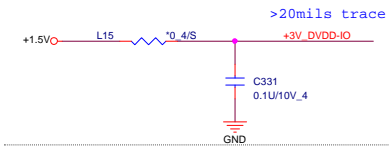
| CN table | |
|----------|------------|
| 1 | AGND |
| 2 | AVDD2.8V |
| 3 | NC |
| 4 | D0VDD1.8V |
| 5 | DGND |
| 6 | XVCLK |
| 7 | DGND |
| 8 | RESETB |
| 9 | SIO D |
| 10 | SIO C |
| 11 | PWDN |
| 12 | NC |
| 13 | NC |
| 14 | DGND |
| 15 | MIPI CLK P |
| 16 | MIPI CLK N |
| 17 | DGND |
| 18 | MIPI DI P |
| 19 | MIPI DI N |
| 20 | DGND |

| EN1, EN2 | | | | | | |
|------------------------|----------------|--------------------|-----|-----|-----|--|
| Enable Input Threshold | V _H | Regulator enabled | 1.5 | --- | --- | |
| | V _L | Regulator shutdown | --- | --- | 0.5 | |

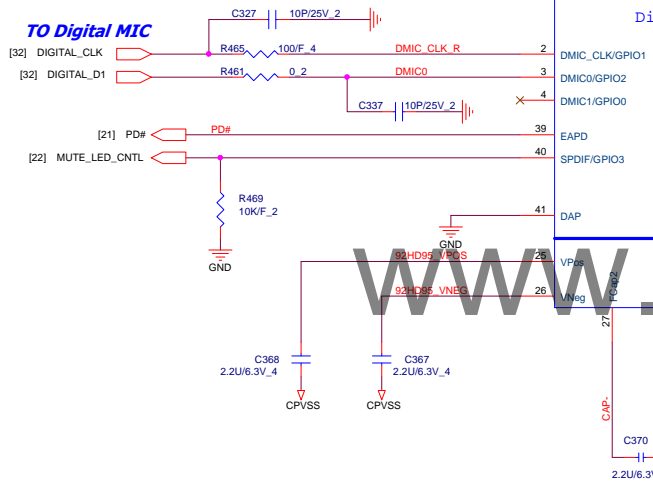


PROJECT : W03Z
Quanta Computer Inc.

| | | |
|--------------------------------|---|----------------|
| Size Custom | Document Number Front/Rear Camera Module | Rev 1A |
| Date: Wednesday, July 31, 2013 | | Sheet 19 of 44 |

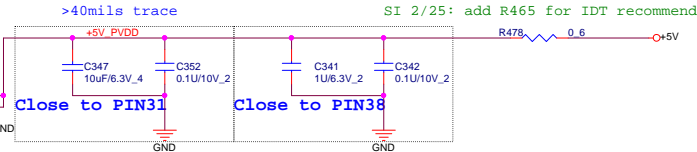
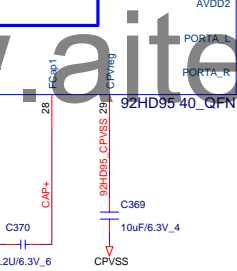


TO Digital MIC



Digital Analog

ClassG Area

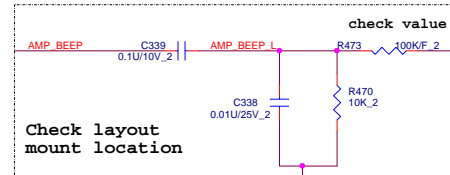


COMPONENT CHOICES ON FERRITES:

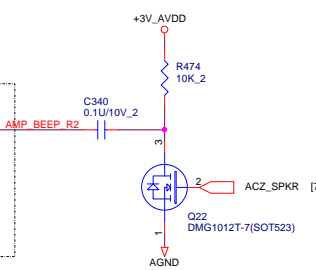
Ferrites are only necessary when required by EMI.

The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements. At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:

Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T

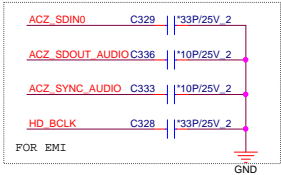
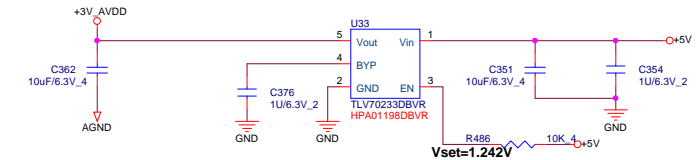
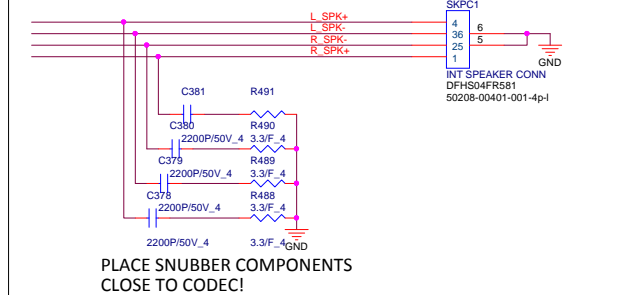


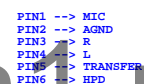
Check layout mount location



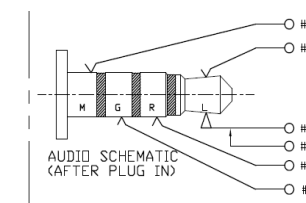
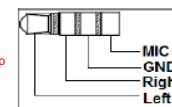
Speaker 4 ohm: 40mils

Speak conn.

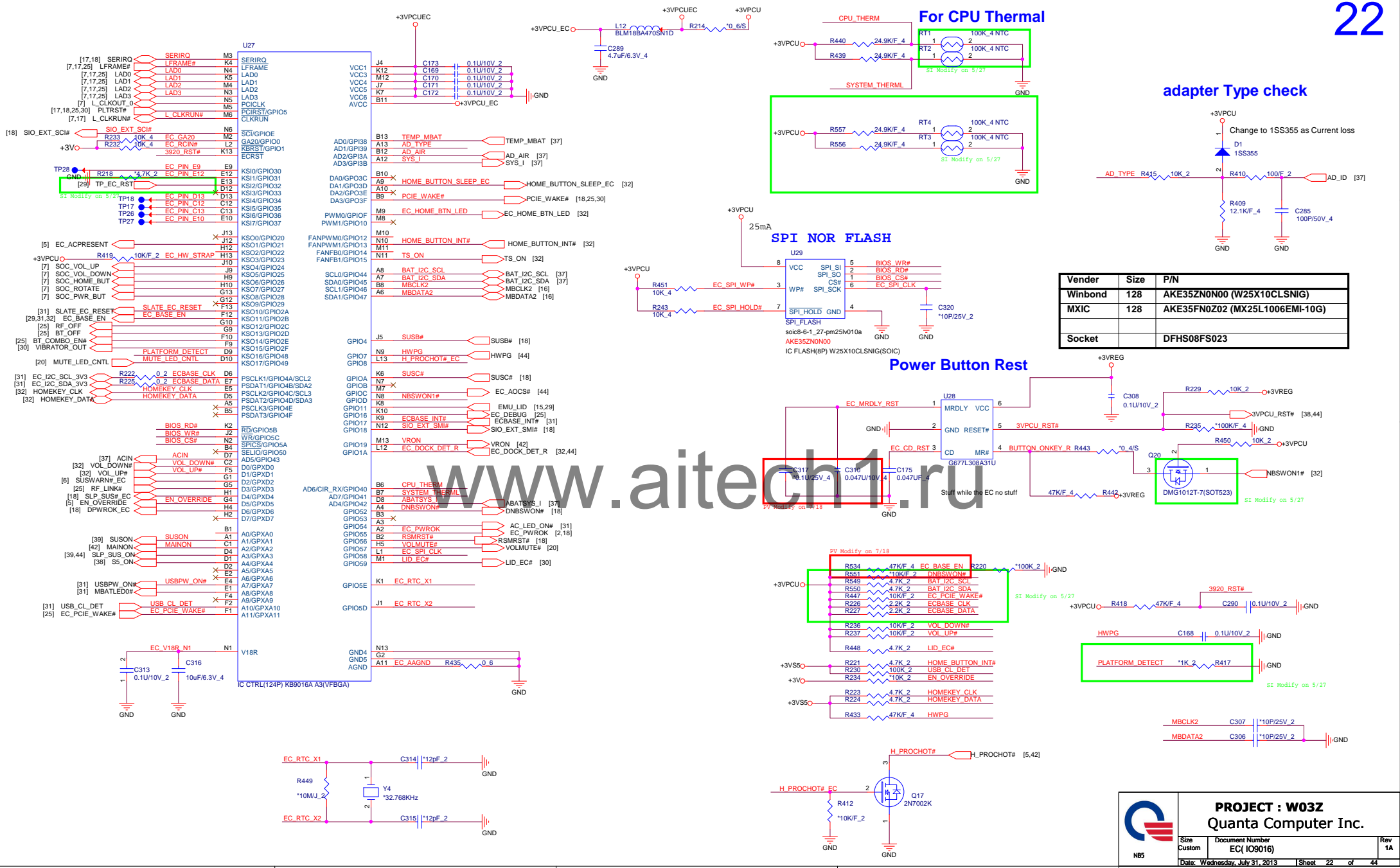




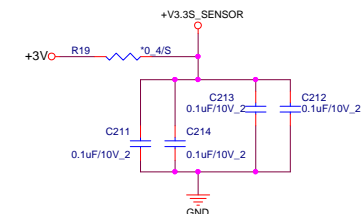
Audio combo Jack



Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T



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PV Modify on 7/18

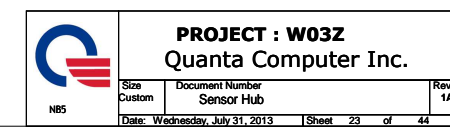
I2C 1 SCL HUB 3P3
I2C 1 SDA HUB 3P3
I2C 4 SCL HUB 3P3
I2C 4 SDA HUB 3P3

SENSOR_HUB_WAKE_LS
ALS_INT_N

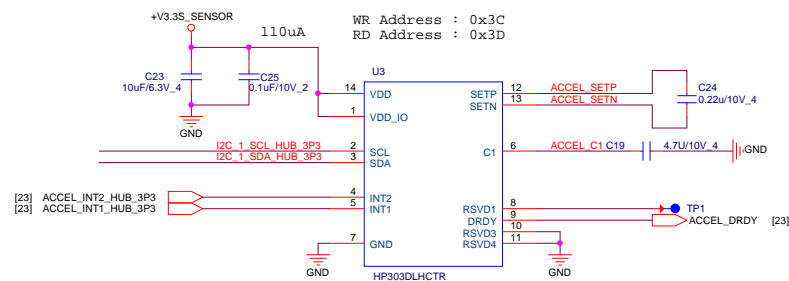
R304 2.2K 2
R303 2.2K 2
R302 2.2K 2
R27 2.2K 2
R298 10K 2
R300 10K 2

+V3.3S_SENSOR
PB13
R25 10K 2
GND

www.aitech1.ru To SoC



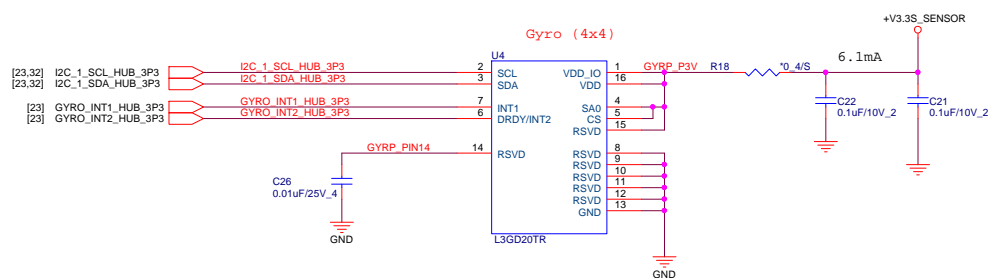
G-sensor/E-compass




www.aitech1.ru

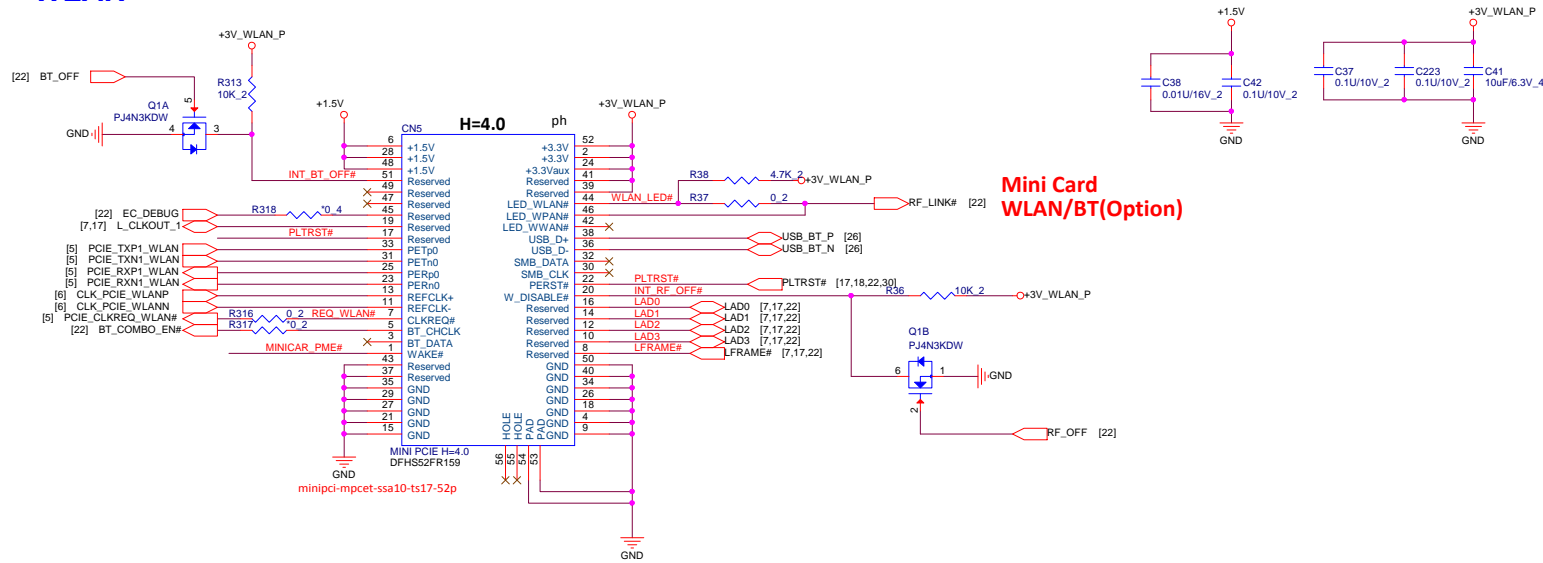
Gyroscope

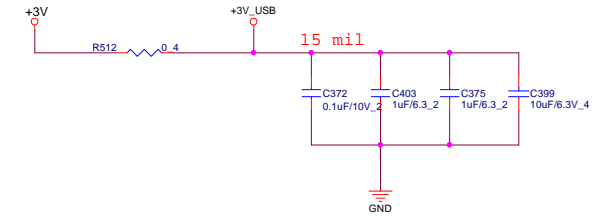
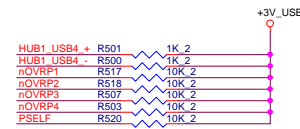
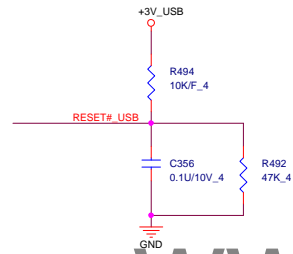
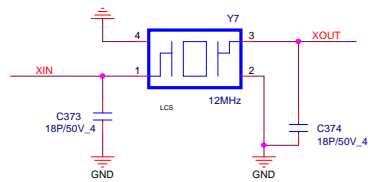
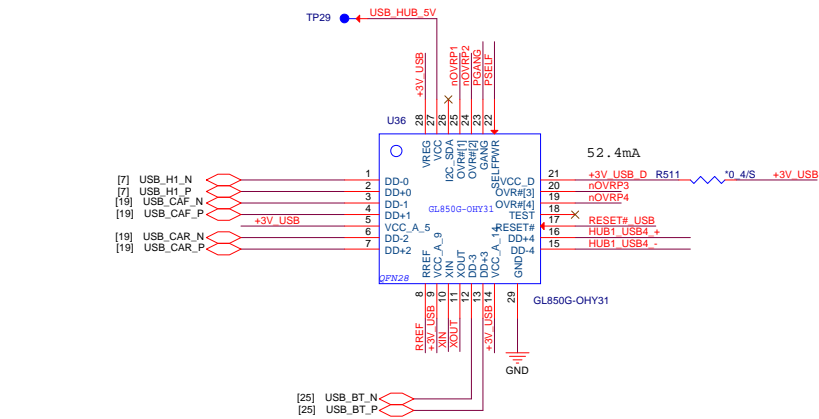
WR Address : 0xD2
RD Address : 0xD3



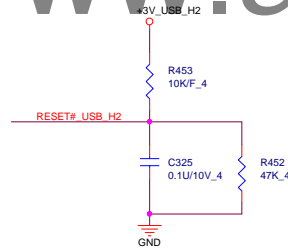
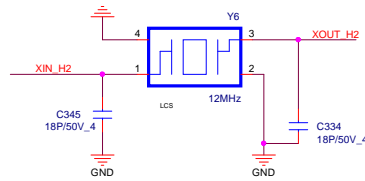
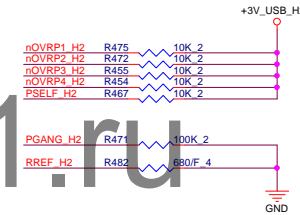
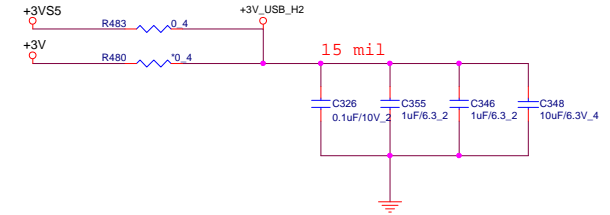
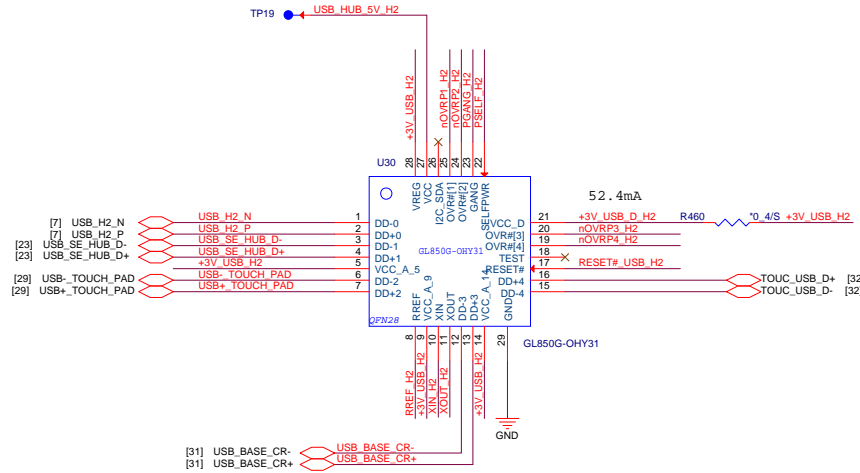
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|--|--|------------------------------------|-----------|
|  NB5 | PROJECT : W03Z Quanta Computer Inc. | | |
| | Size Custom | Document Number G-Sensor / Gyro | Rev 1A |
| | Date: Wednesday, July 31, 2013 | Sheet 24 of 44 | 1 |

WLAN





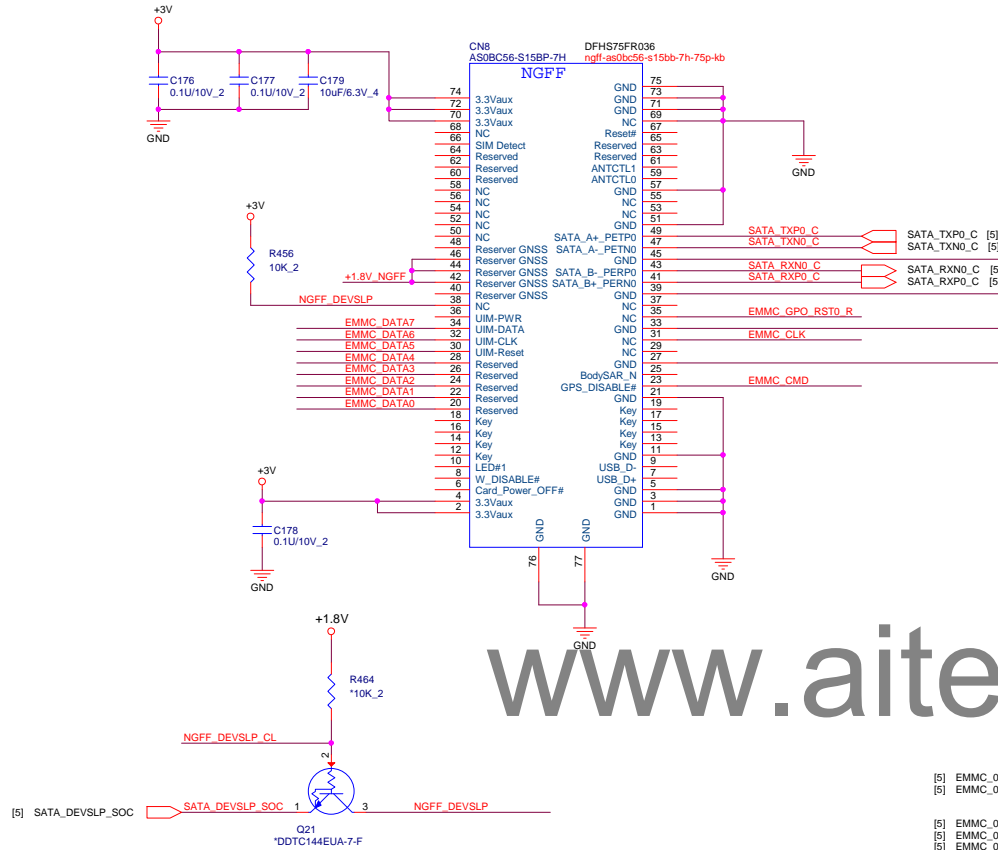
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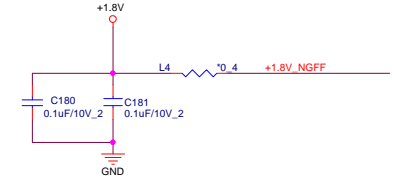
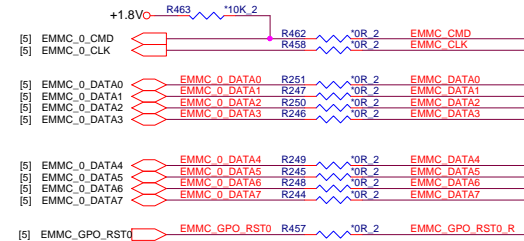
www.aitech1.ru

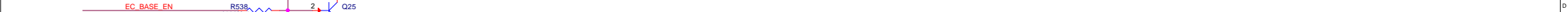
SSD (NGFF Connector)

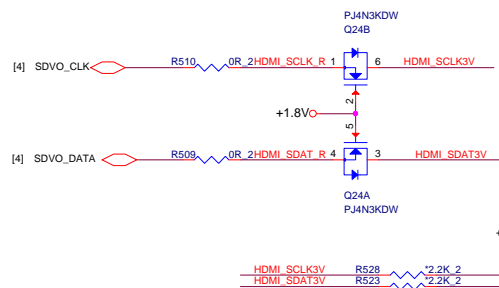
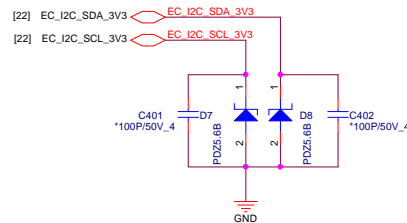
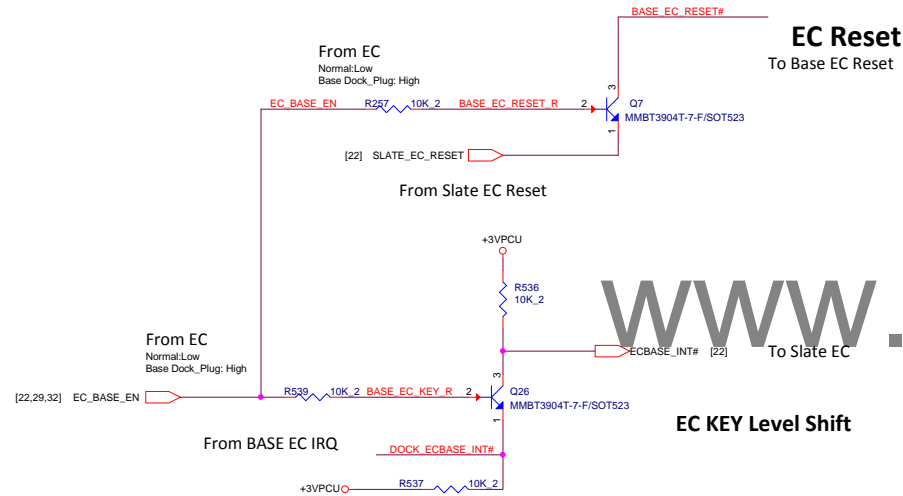
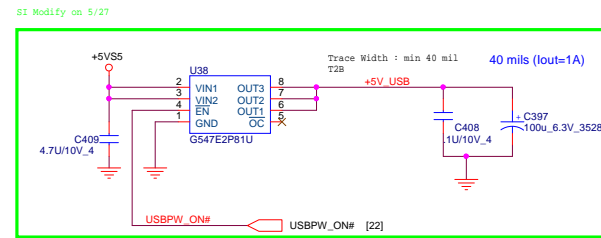
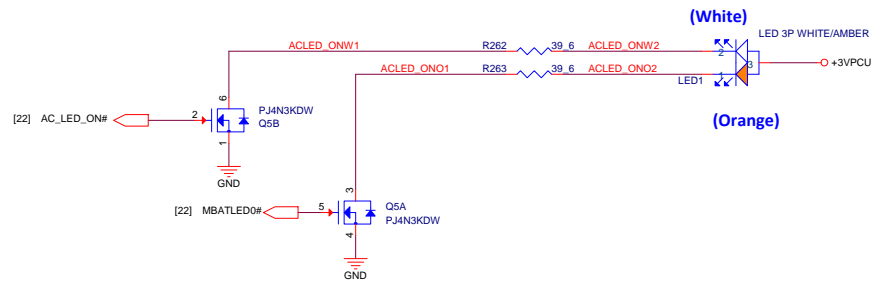
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Base Left side USB 2.0

Card reader

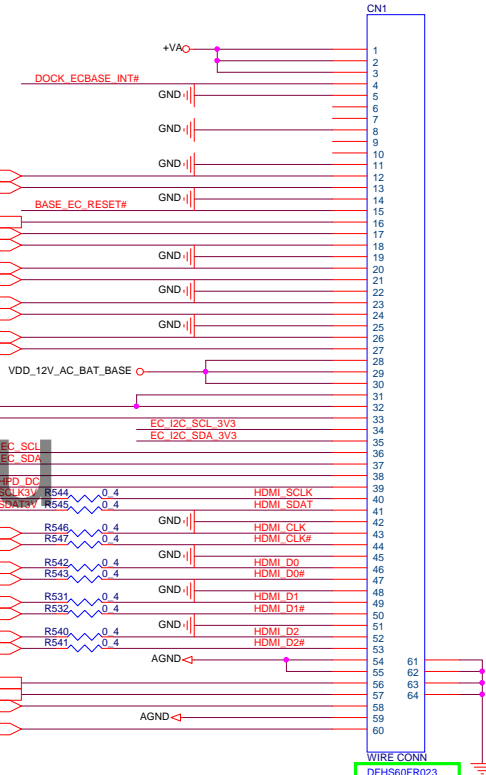
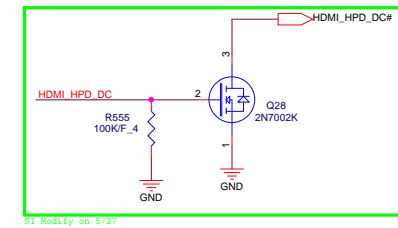
Base Right side USB 3.0

USB dongle Cable power

Touch PAD I2C

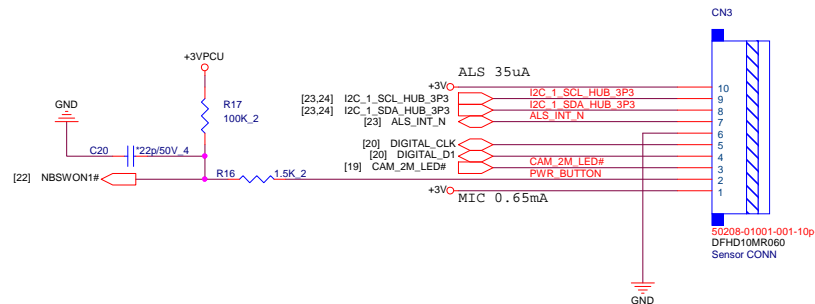
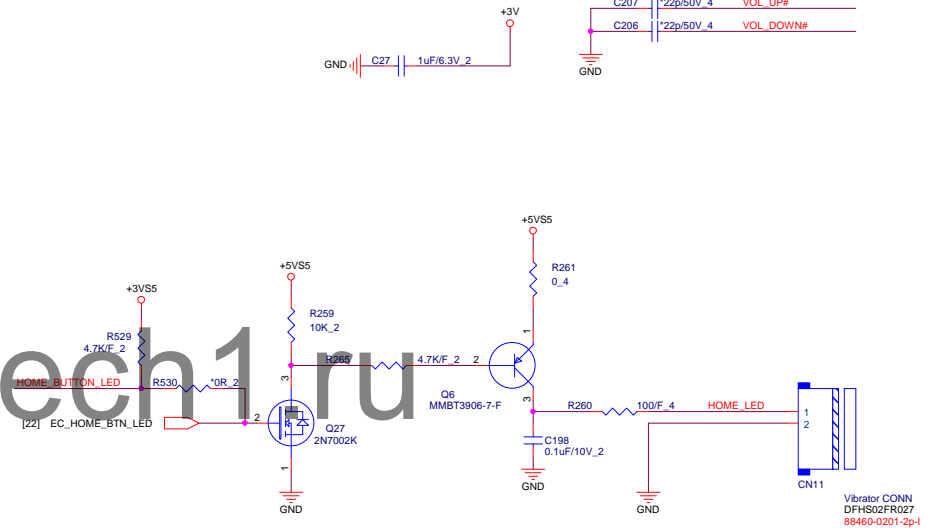
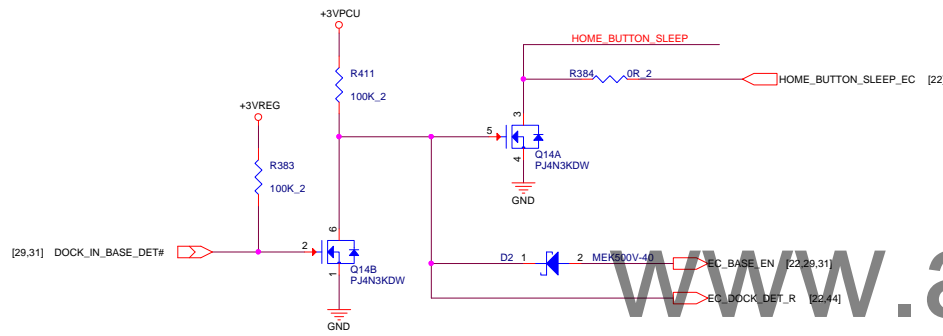
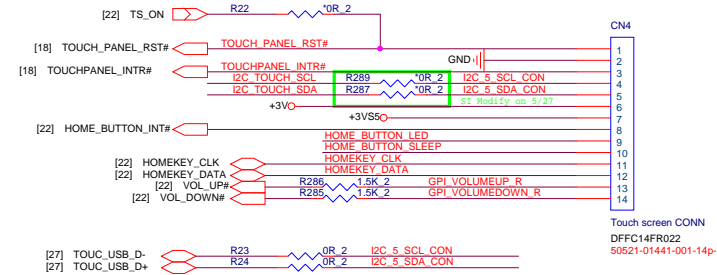
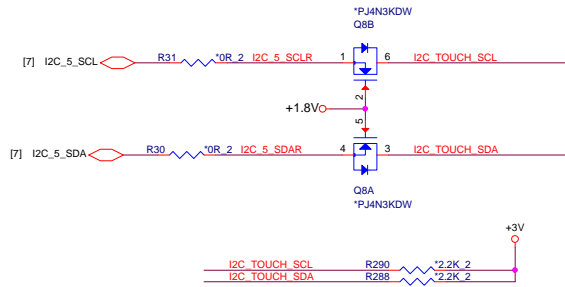
HDMI

Audio




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Quanta Computer Inc.


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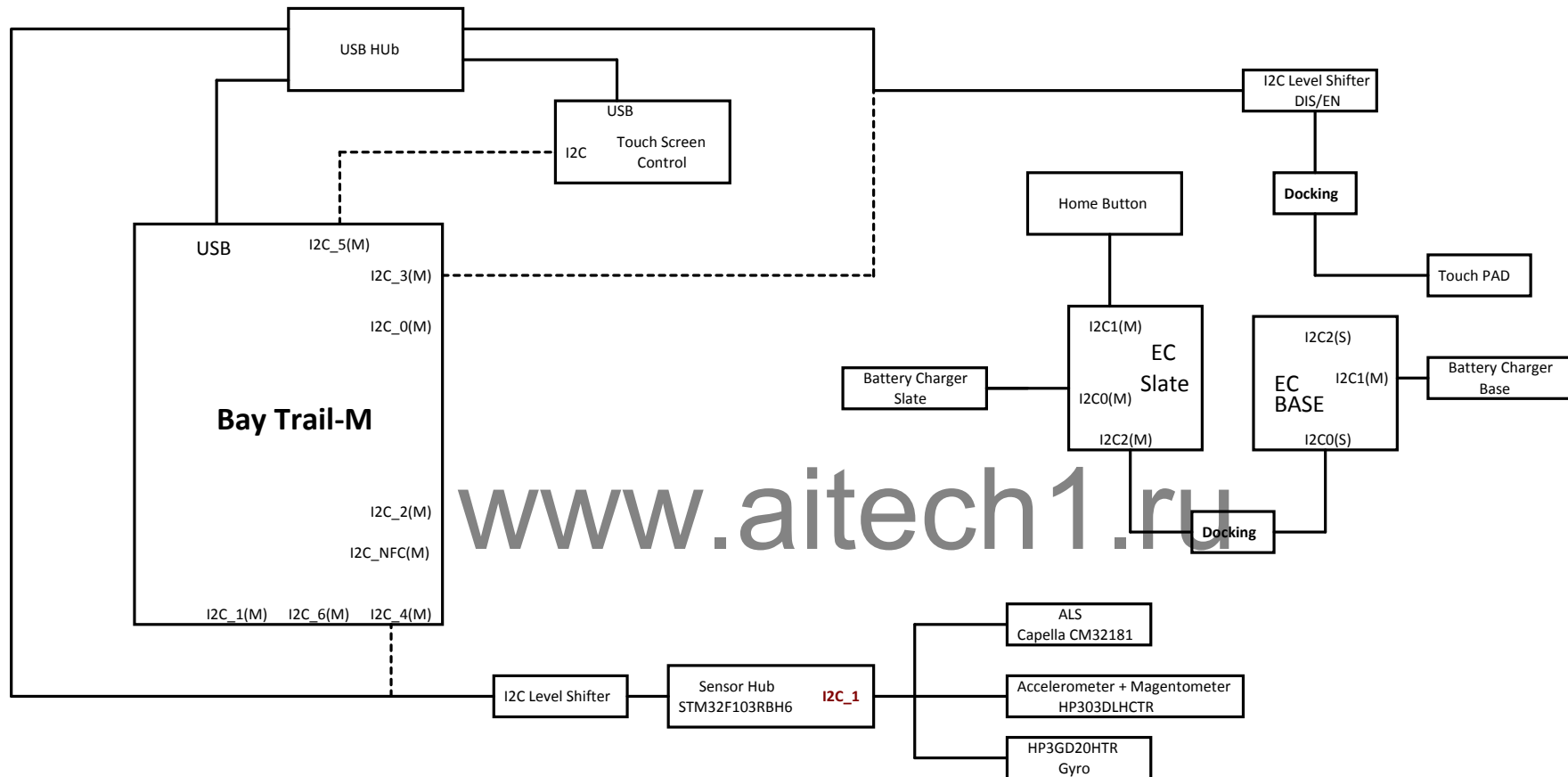


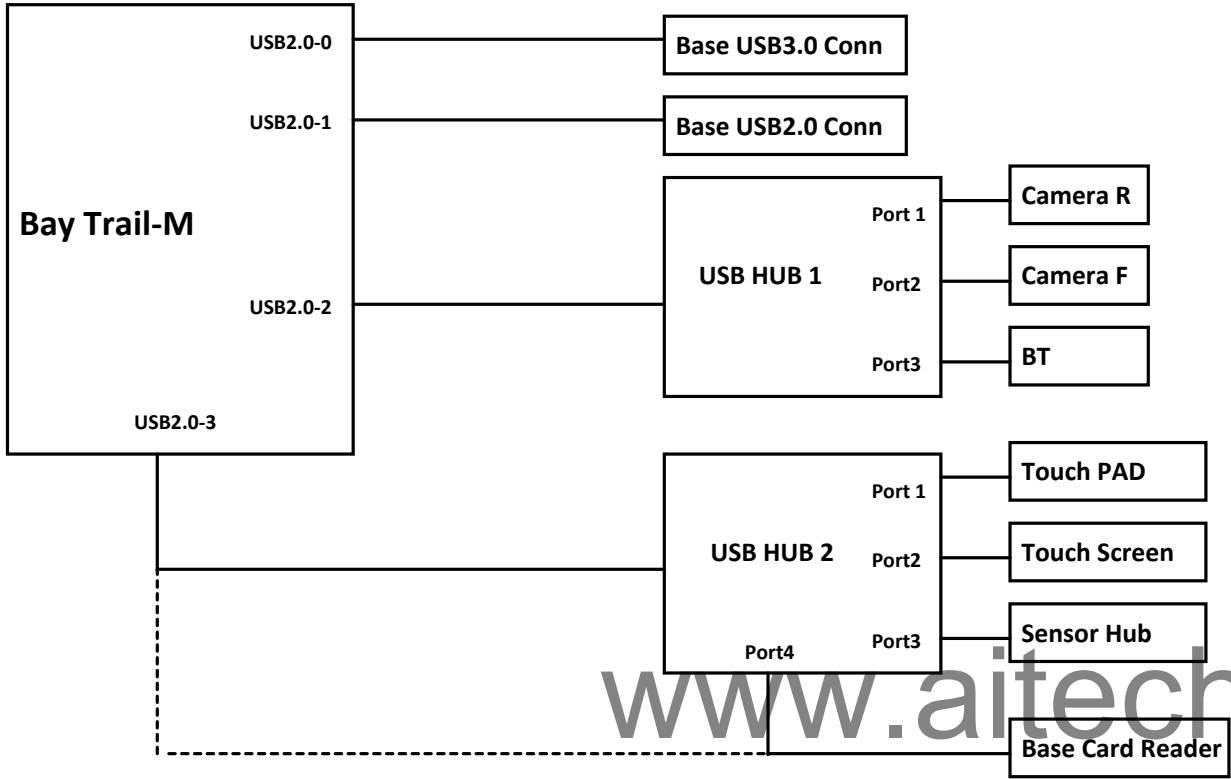
PB + ALS + DMIC + WEBCAM LED CONNECTOR

| | | | |
|---|--------------------------------|----------------------------------|--------|
|  | PROJECT : W03Z | | |
| | Quanta Computer Inc. | | |
| | Size Custom | Document Number SMALL BOARD CONN | Rev 1A |
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|  NB5 | PROJECT : W03Z Quanta Computer Inc. | | |
| | Size Custom | Document Number NA | Rev 1A |
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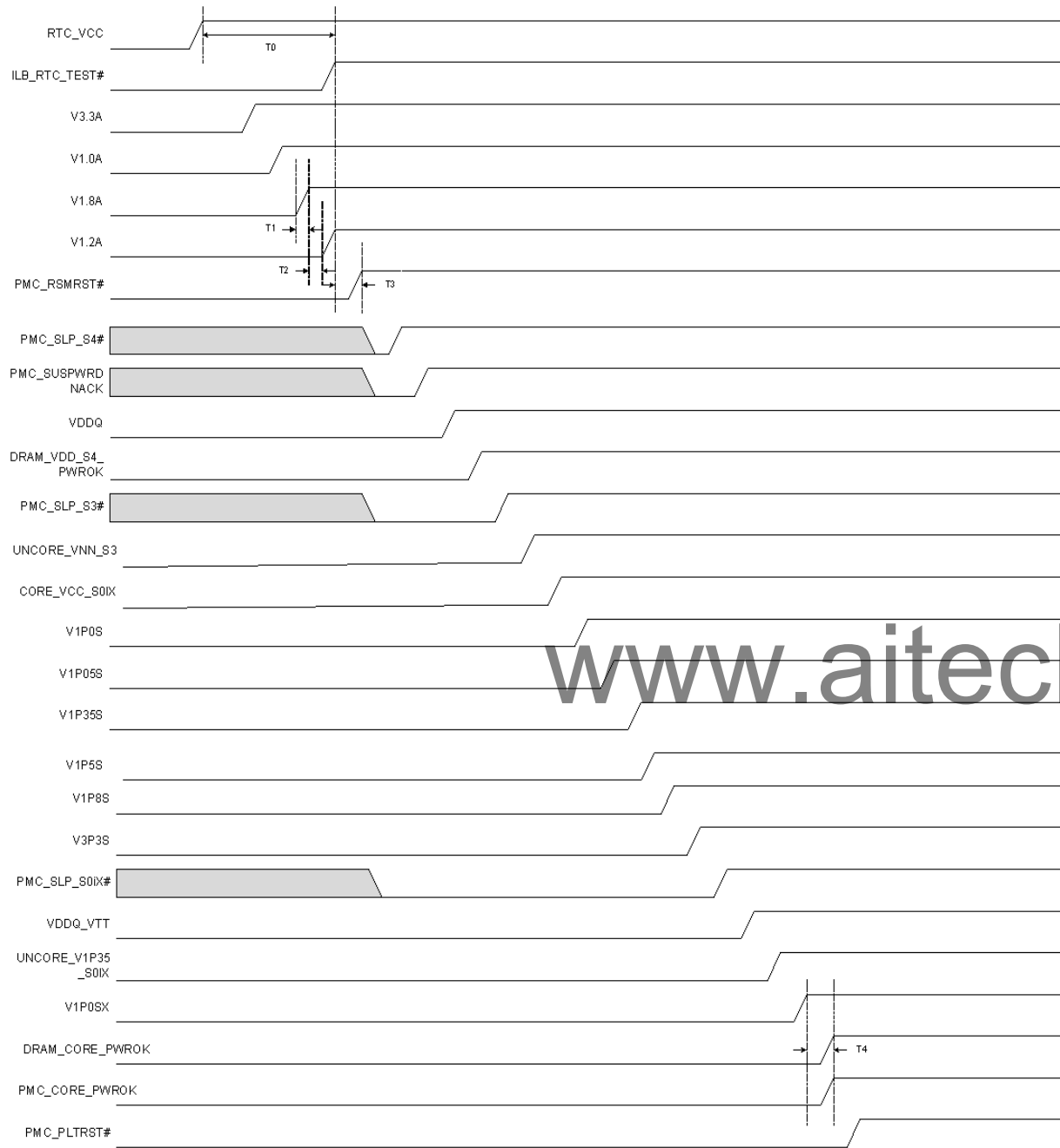


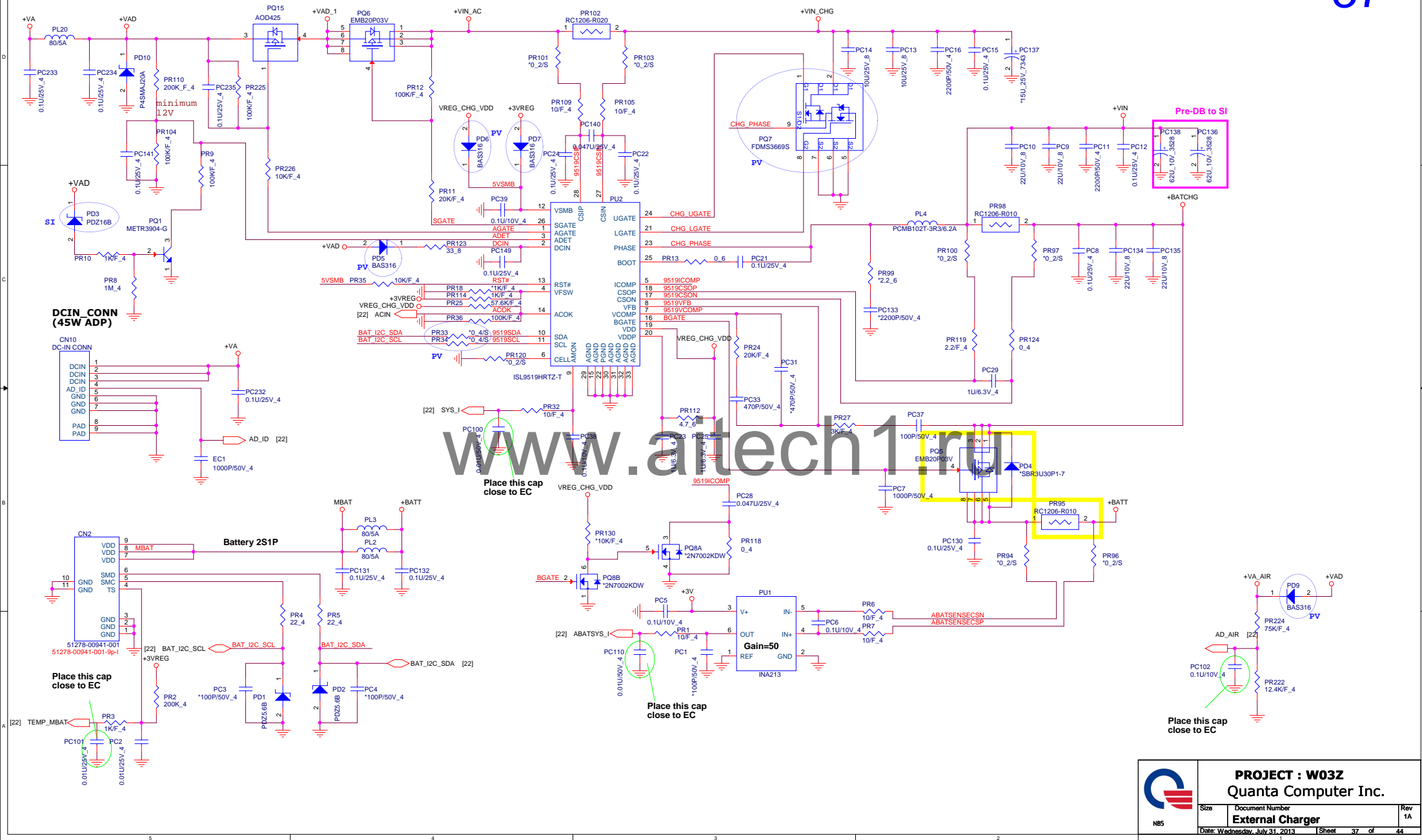
Table 4-12. Cold Boot Timing Spec

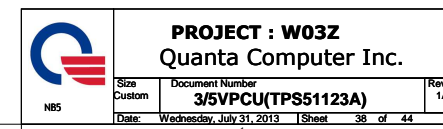
| Parameter | Description | Min | Typ | Max | Units |
|-----------|---|-----|-----|------|-------|
| T0 | RTC_VCC stable to ILB_RTC_TEST# high | 9 | | | ms |
| T1 | VR ramp up time from 10% to 90% voltage level | | | 2 | ms |
| T2 | Rail to subsequent rail turn on delay | 10 | | 2000 | us |
| T3 | VSUS stable to PMC_RSMRST# high | 10 | | | ms |
| T4 | S and SX rails stable to PMC_CORE_PWROK | 100 | | | ms |

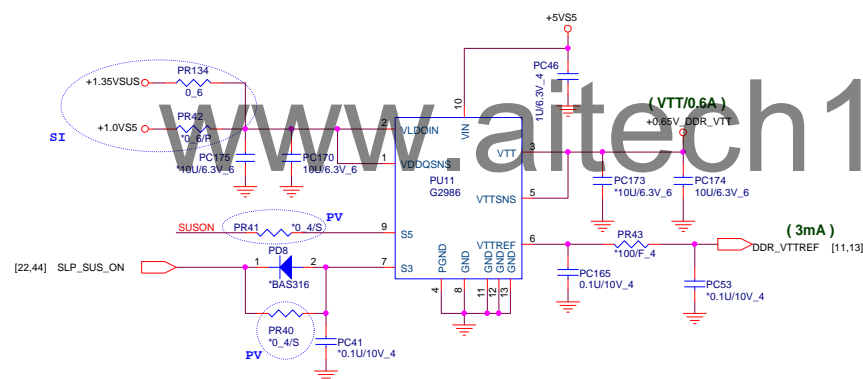
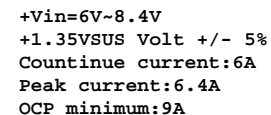
NOTES:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.
2. Violation of rail-to-rail sequencing may cause the SoC part long term reliability issue.
3. Platform devices other than SoC sequencing are not explicitly shown as they are not limited by the SoC sequencing requirement.

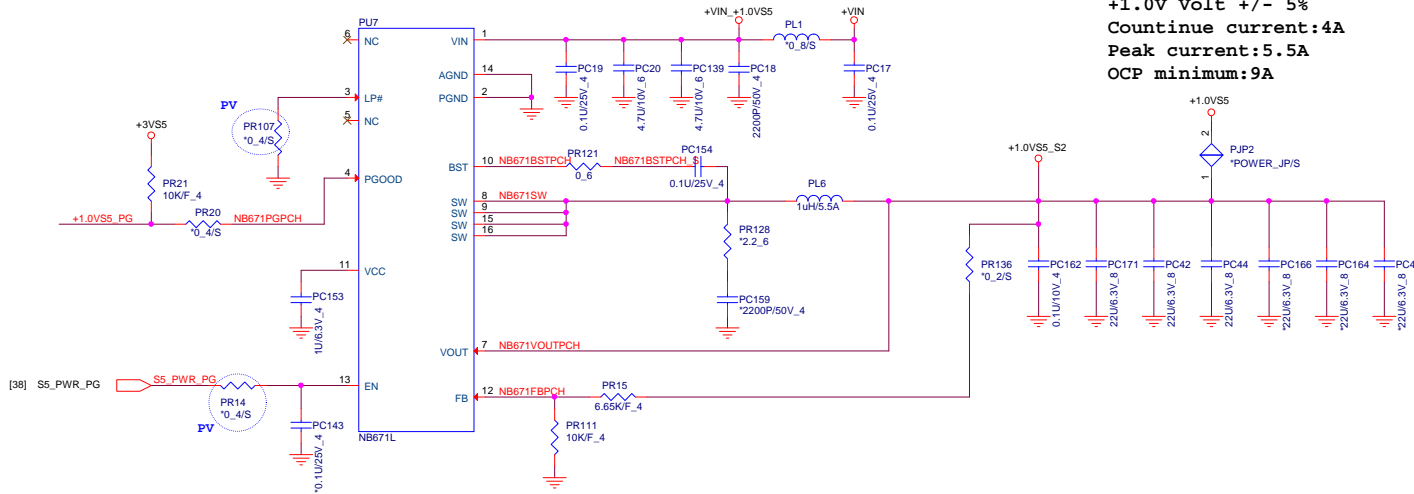
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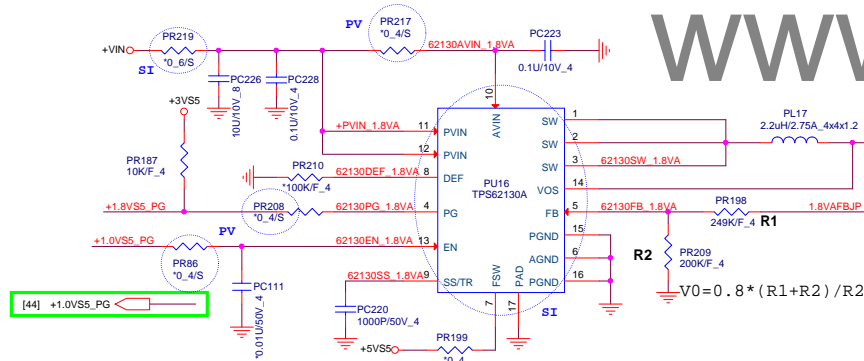
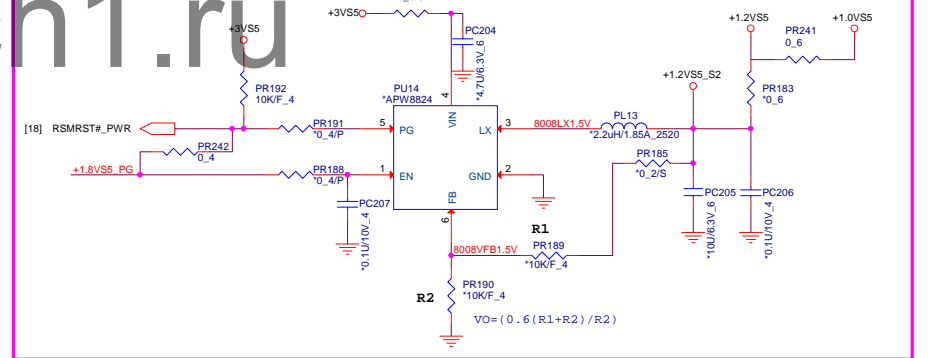
+Vin=6V~8.4V
+1.0V Volt +/- 5%
Countinue current:4A
Peak current:5.5A
OCP minimum:9A



+Vin=6V~8.4V
+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

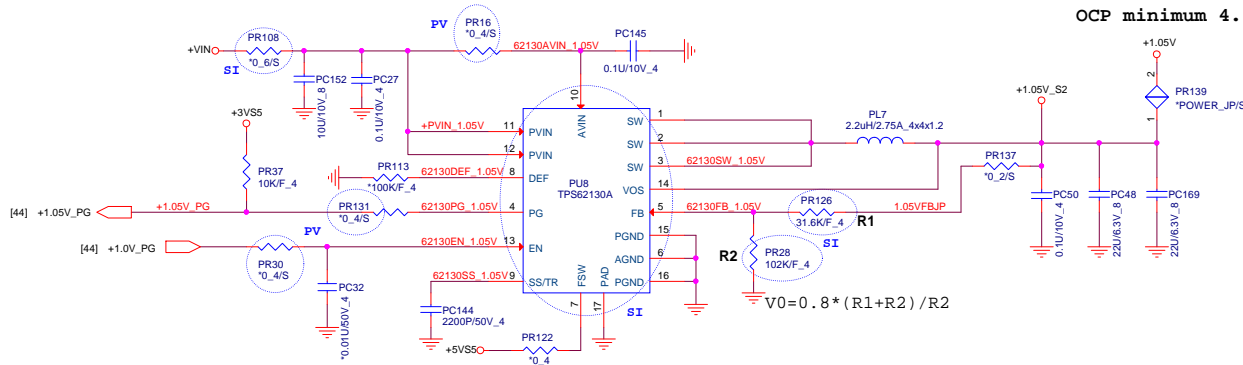
Pre-DB to SI
SI to PV

+1.2V +/- 5%
Countinue current:0.5A
Peak current:1A
OCP minimum 1.45A

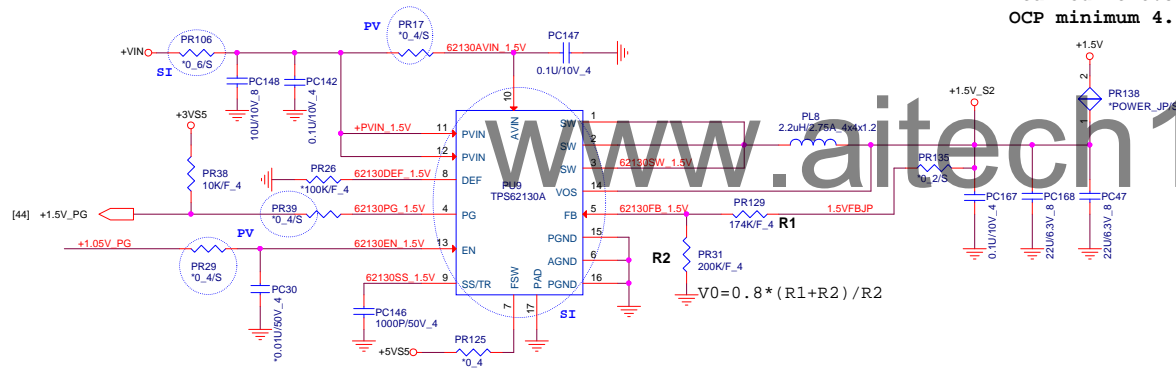


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+Vin=6V~8.4V
+1.05V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

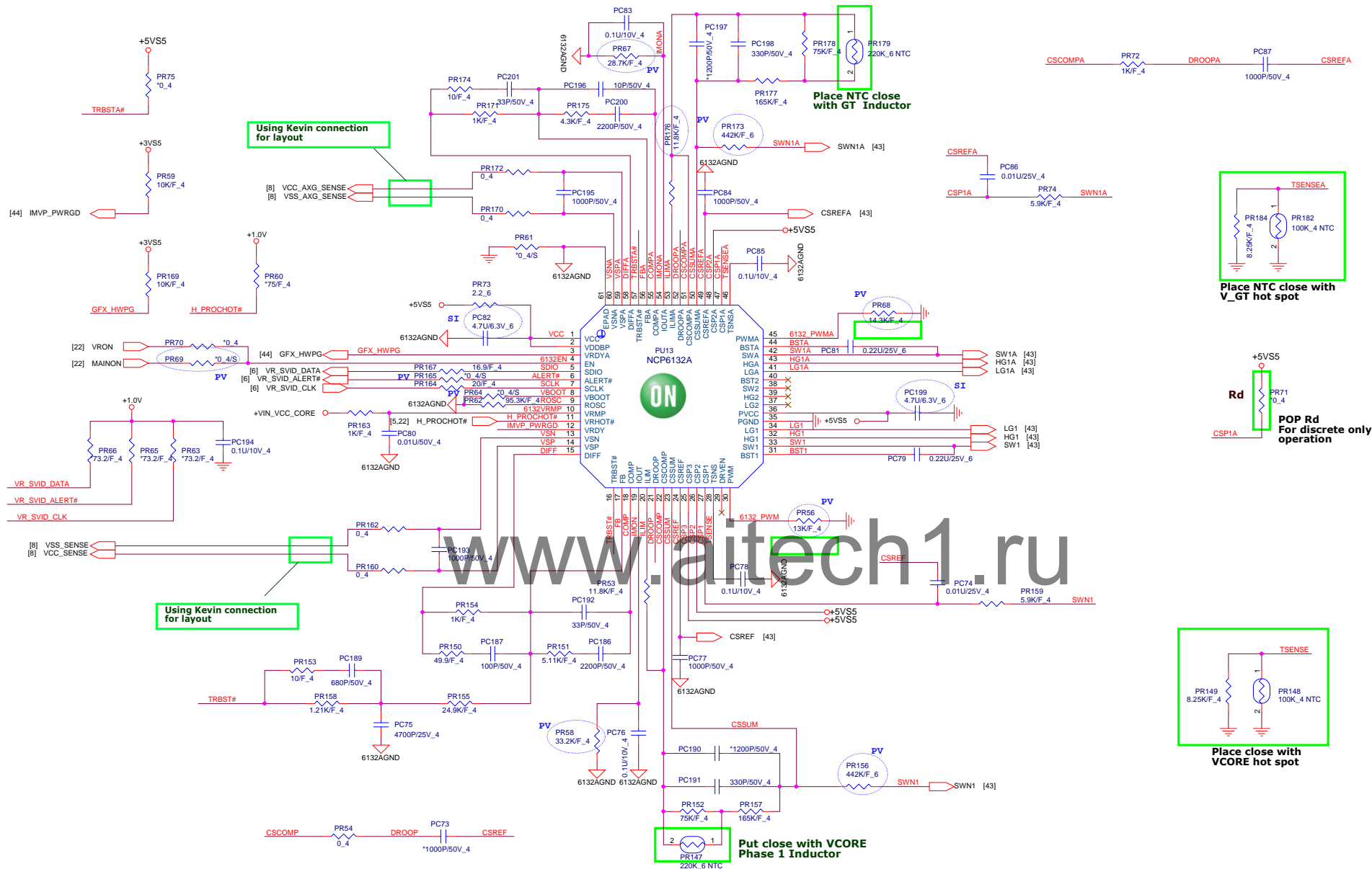


+Vin=6V~8.4V
+1.5V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A



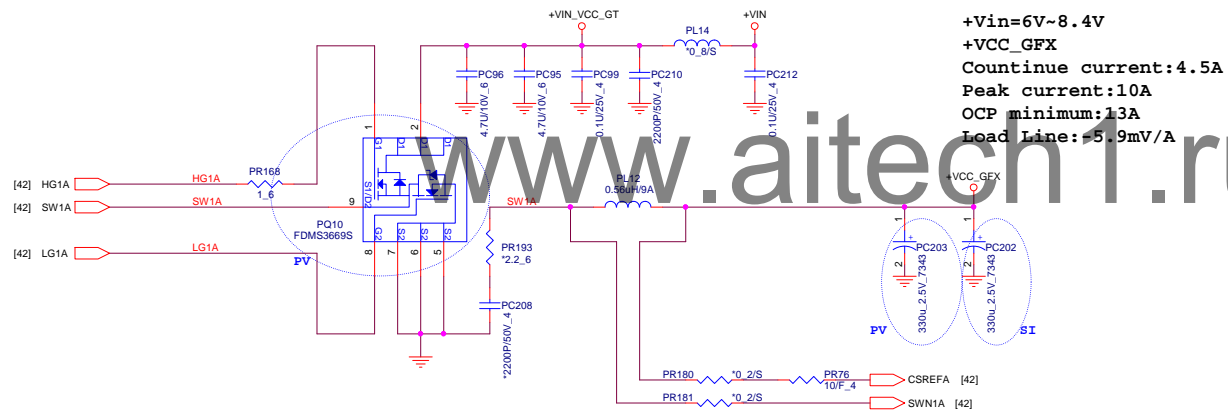
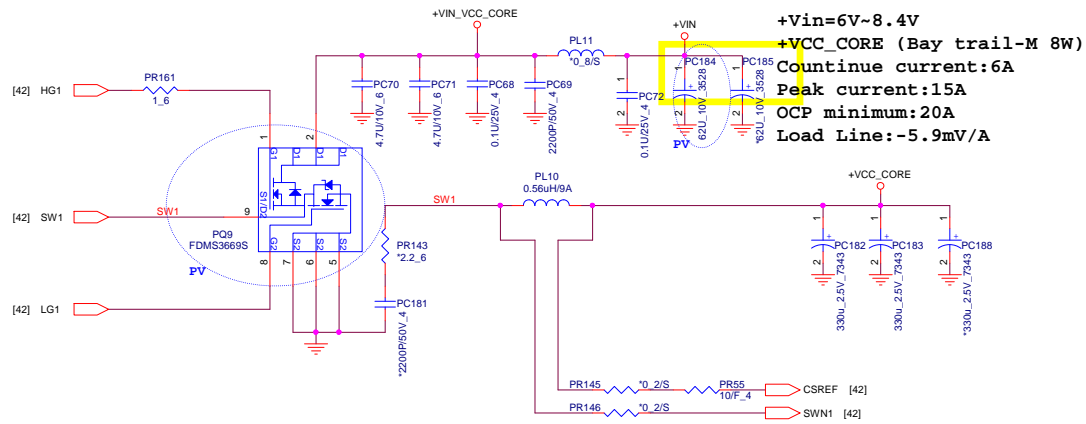
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|--------------------------------|---|-----------|
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| Custom | CPU Core1 (NCP6132B) | 1A |
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| Custom | CPU Core2 (NCP5911) | 1A |
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